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FPGA BASED COMPENSATION METHOD FOR CORRECTING DISTORTION IN VOLTAGE INVERTERS

by

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December 2007

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This thesis presents a method to compensate for the blanking time distortion in Space Vector Modulated (SVM) voltage source inverters. Blanking time distortion is caused by the delay inserted to prevent the short circuit that would occur if the two transistors in the same inverter leg are both on at the same time. This delay produces harmonic distortion and non-linearity when two-switch phase legs are used in inverters to generate sinusoidal voltages for various types of AC loads. The approach in this thesis uses a Field Programmable Gate Array to create a pulse by pulse compensation technique that adjusts the symmetric SVM pulses in an attempt to eliminate the voltage distortion caused by the blanking time effect. This technique is evaluated through simulation and experimental results. This thesis proves that the delay caused by the insertion of blanking time can be compensated using a Field Programmable Gate Array and that the blanking time delay is not the dominant source of the 5th and 7th lower order harmonic distortion in voltage source inverters at low voltages.

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FPGA BASED COMPENSATION METHOD FOR CORRECTING DISTORTION IN VOLTAGE INVERTERS

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ABSTRACT

This thesis presents a method to compensate for the blanking time distortion in Space Vector Modulated (SVM) voltage source inverters. Blanking time distortion is caused by the delay inserted to prevent the short circuit that would occur if the two transistors in the same inverter leg are both on at the same time. This delay produces harmonic distortion and non-linearity when two-switch phase legs are used in inverters to generate sinusoidal voltages for various types of AC loads. The approach in this thesis uses a Field Programmable Gate Array to create a pulse by pulse compensation technique that adjusts the symmetric SVM pulses in an attempt to eliminate the voltage distortion caused by the blanking time effect. This technique is evaluated through simulation and experimental results. This thesis proves that the delay caused by the insertion of blanking time can be compensated using a Field Programmable Gate Array and that the blanking time delay is not the dominant source of the 5th and 7th lower order harmonic distortion in voltage source inverters at low voltages.

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EXECUTIVE SUMMARY

This thesis explores a method to compensate for the output voltage distortion in pulse width modulated (PWM) voltage source inverters (VSI) caused by the delay inserted to prevent the short circuit that would occur if the two transistors in a single inverter leg were both on at the same time. This distortion is often referred to as blanking time or dead time distortion. This thesis utilizes a pulse based compensation method to compensate for the distortion. The need for the blanking time delay is explored by an examination of a single leg of a VSI as illustrated in Figure 1.

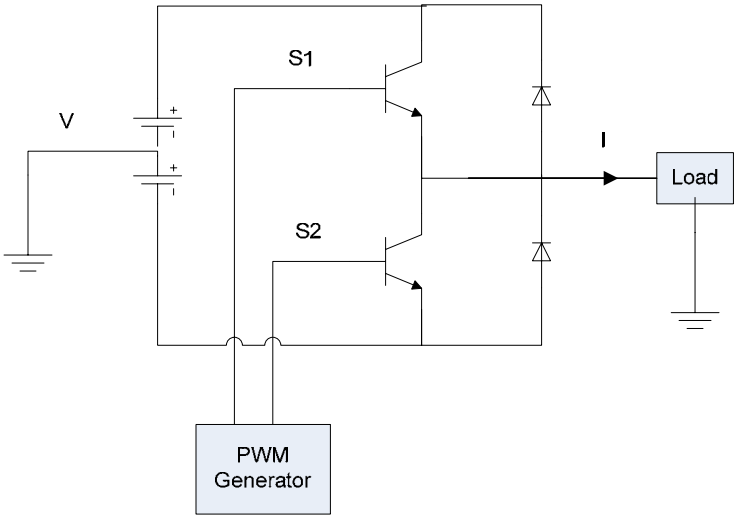

Figure 1. Single Voltage Source Inverter Leg.

In ideal voltage source inverters the switching of individual inverter legs is assumed to be perfect, which allows the state of the two switches in an inverter leg to change simultaneously from on to off and vice versa. In reality there is a finite turn-off and turn-on time associated with any transistor. If both transistors in an inverter leg are on at the same time, a short circuit occurs. Blanking time is inserted to delay the turn on of the second switching device until the first has turned off. This delay, which is inserted to protect the device, creates distortion. The compensation method explored in this thesis uses a single Field Programmable Gate Array chip, the Virtex II^{TM}, to implement a pulse by pulse compensation technique that adjusts the symmetric PWM pulses in an attempt to

eliminate the voltage distortion caused by the blanking time effect. The technique uses the polarity of the output current to determine when to insert a delay to the PWM signal and create a uniform delay between the gate signal and the output voltage waveform, v_{AN}. The compensation method is illustrated in Figure 2.

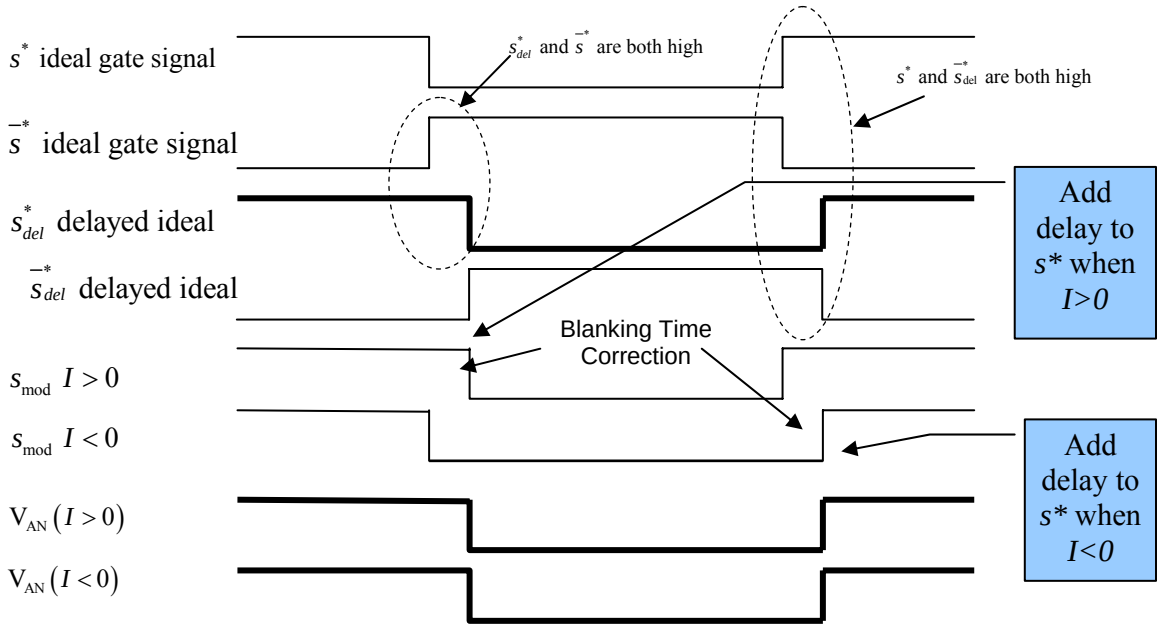

Figure 2. Blanking Time Compensation Technique.

When the current polarity is positive the gate driver signal, s^*, is modified as shown in Figure 2. Turning off the transistor, S1, will immediately cause the output voltage to transition from $+V_{DC}/2$ to $-V_{DC}/2$ when the current is positive. Inserting a falling edge delay as shown in the modified gate signal in Figure 2 compensates for the blanking distortion when the current is positive.

When the current polarity is negative the rising edge of the ideal gate signal, s^*, is delayed as shown in Figure 2. The rising edge is delayed because when the current is negative transistor S2 in Figure 1 will turn off immediately if a delay is not added.

A SIMULINK® model was created to simulate a VSI and predict the output voltage. The simulated results confirm that the compensation method presented in this thesis effectively neutralizes the distortion caused by blanking time. Experiments were then conducted; the results from the experiments showed the delay in the switching

pattern was uniform after compensation, and thus the blanking time delay had been compensated for. The output voltage spectrum however, did not correspond with the simulated results. The output voltage spectrum did not improve after the creation of a uniform delay. The lower order harmonics, primarily the 5^{th} and 7^{th}, were still present in the output waveform. This leads to the conclusion that the blanking time delay can be compensated for by a pulse based approach but the distortion caused by blanking time is not the most dominant source of distortion in SVM controlled voltage source inverters.

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I would like to thank my advisor, Professor Alex Julian for his guidance in this thesis research. He always had suggestions and new ideas when I ran into problems with the modeling of the system, and his help in understanding the hardware was invaluable. I would like to thank my Second Reader Professor Cristi for all the help he gave me on my introduction and background information. One of my fellow students also deserves to be recognized. Stephen Blevins was always willing to help out with brainstorming, troubleshooting, and coding. I would like to thank my two moms for the love and support they have given me. Last but definitely not least, I would like to thank my wife for her love, support, and understanding through all the years we have been married, she makes me better.

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I. INTRODUCTION

A. BACKGROUND

Modern motor control provides variable voltage and frequency to the inputs of the motor through a pulse width modulated (PWM) voltage source inverter drive. The choice of the PWM strategy is important to reduce the voltage and current harmonics produced by the PWM algorithm. Fast switching devices in power inverters such as metal-oxide-semiconductor field-effect transistors (MOSFETs) or insulated gate bipolar transistors (IGBTs) do not switch on/off instantaneously. In order to prevent a short circuit, a delay in the rising edge of each transistor gate signal is introduced. This blanking time, also referred to as dead time, is the small time delay inserted to prevent a short circuit in an individual inverter leg. A single leg of a VSI is illustrated in Figure 3.

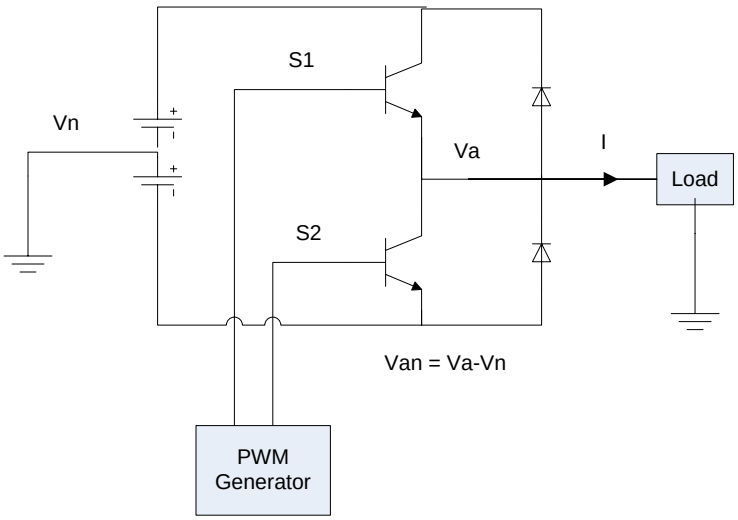

Figure 3. Single Inverter Leg.

In ideal voltage source inverters the switching in individual legs is assumed to be perfect, which allow the status of the two switching devices in an inverter leg to change simultaneously from on to off and vice versa. In reality there is a finite turn-off and turn-on time associated with any transistor. If both transistors in an inverter leg are on at the same time a short circuit occurs. A delay is inserted to postpone the turn on of the second switching device until the first has transitioned off.

Although the blanking time delay is relatively short, it causes errors in the desired output voltage. Each error individually does not substantially affect the fundamental output voltage; the accumulation of these errors can result in a reduction of the fundamental output voltage and torque pulsations [1]. The problem has been investigated by industry and several methods of correction have been proposed [2].

Correctly compensating for the effects caused by blanking time distortion has advantages. Industrial applications such as the ac induction motor in a fan or a pump, or the ac synchronous reluctance motor used in textile applications would benefit from better and more effective PWM schemes. Blanking time distortion also causes machine losses and lowers efficiency. If the PWM strategy is not effectively implemented it could produce excessive harmonics. Other authors have noted that the system stability will also be affected by these harmonics, especially at low frequencies and no-load conditions causing additional machine losses. The magnitude of these losses will depend on the magnitude of the harmonic content in the applied voltage. Excessive harmonics can increase motor temperature and cause torque pulsations [1].

B. OBJECTIVE AND APPROACH

The objective of this thesis is to develop a method to compensate for the delay and distortion associated with blanking time in the Semikron SemiTeach IGBT using SIMULINK® software embedded in an FPGA. The performance of the ideal VSI system, the VSI system with blanking time distortion, and the system with the compensation is analyzed to determine the effectiveness of the purposed method. The compensation method is then tested in the laboratory and the results are compared with the simulation results. A custom printed circuit board is utilized to interface the FPGA with the Semikron IGBT in order to test the compensation method.

The compensation method is based upon adjusting the PWM pulses to correct for the delay caused by blanking time. The VSI PWM control method was created in MATLAB® using the SIMULINK® modeling tool and was provided in [6]. Using XILINX® developments tools the SIMULINK® model is converted into VHDL programming code. This code is imbedded into the Virtex II™ FPGA which generates the PWM scheme and provides the gate signal inputs to the SemiTeach IGBT. The entire

system was modeled in SIMULINK® and the compensation method was implemented via simulation. Laboratory experiments compare the delay between the actual gate driver signals and corresponding output voltage signal prior to compensation. These results are compared to the delay between the same two signals after the compensation method is implemented to determine the effectiveness of the compensation code. In order to establish the overall impact of the compensation code the Total Harmonic Distortion (THD) of the system prior to compensation will be compared to the THD of the system after blanking time distortion compensation. These results will be analyzed and compared to the simulation to determine the value of the compensation method.

C. RELATED WORK

The subject of waveform distortion due to the blanking time, sometimes referred to as "dead time", has received considerable attention in the literature. The distortion of the voltage waveform was described by Murai in [3], and the instability caused by the blanking time was described by Ueda and Sonoda in [4]. Other authors have discussed various other methods for correcting blanking time distortion. Colby, *et al*. in [5] presented a corrective measure that adds an offset to the reference signal which corrects the dc offset introduced by the blanking interval. The compensated reference signal cancels the error introduced by the blanking interval and therefore should reduce the waveform distortion. This compensation was implemented in software in a microprocessor controlled PWM inverter [3]. Another method for compensation was proposed by Munoz *et al*. in [2]. In this approach the basic principle is to compensate for the average loss or gain of voltage per carrier period, which is based on the instantaneous average voltage method. In the previous compensation method [2] the author did not use the more accurate pulse based compensation approach utilized in this thesis. A Digital Signal Processor, which lacks the processing power of a FPGA, was used to implement the system in [2]. The author mentions the desire to implement a pulse based approach but the increased overhead on the DSP would not allow it.

D. THESIS ORGANIZATION

This thesis is organized as follows Chapter I is an overview of the research effort and the layout of the thesis.

Chapter II introduces the theory behind and problems associated with blanking time distortion. This chapter also presents the design and construction of the blanking time compensator using a computer model.

Chapter III presents the computer model of the entire system and the simulation results.

Chapter IV provides an overview of the hardware utilized in this research.

Chapter V presents the experimental results from the laboratory. The compensator's performance is also analyzed.

Chapter VI provides conclusions and future research opportunities.

Appendix A contains pertinent computer code and SIMULINK® models.

Appendix B contains photos and the schematic for the interface board.

II. COMPENSATION DESIGN METHOD

A. OVERVIEW

This chapter describes the overall system model and the design and construction of the blanking time compensator XILINX® blocks. The SIMULINK® modeling tool was used to mathematically model the system. This chapter is broken into four major sections. The first describes the overall system model. The second provides information concerning blanking time delay. The third explains the method used to compensate for blanking time delay. The fourth section describes how the compensator was constructed using the XILINX® block set.

B. SYSTEM MODEL

The compensator code was added to an existing SIMULINK® Model which produced a PWM control scheme designed for the Semikron IGBT [6]. This code is provided in Appendix A. The PWM control was based on space vector modulation and a schematic of the actual inverter system as shown in Figure 4.

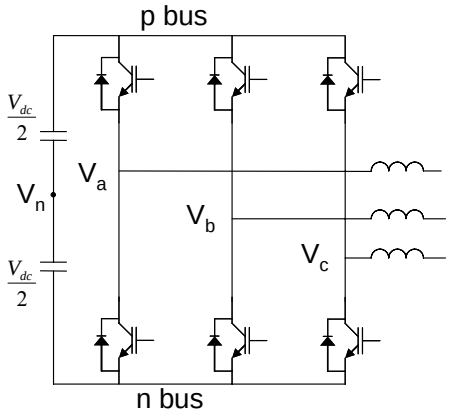

Figure 4. Voltage Source Inverter
From [7].

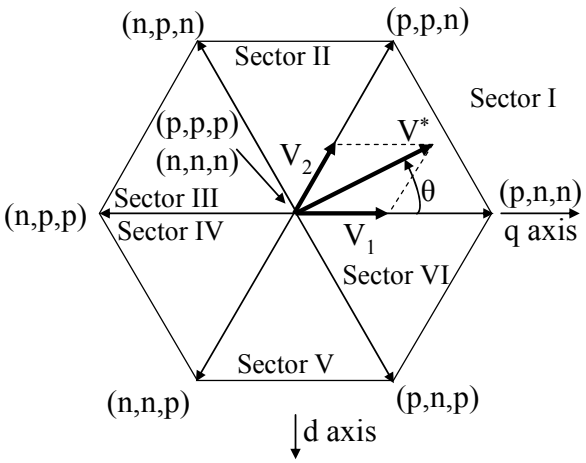

Figure 5. Space Vector Modulation Hexagon
From [8].

The three phase output of the VSI shown in Figure 4 is controlled by modulating the six transistors. The space vector hexagon in Figure 5 shows the **q** and **d** axis voltages for the eight possible switching states. The zero axis voltage is not mapped in Figure 5. The eight states form a hexagon with two zero states mapped to the center of the hexagon. Transformation of the output voltages into the stationary qd0 frame is defined [7].

$$\mathbf{K}_S = \frac{2}{3}\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{-\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.1}$$

$$\begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix} = \mathbf{K}_S \begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} \tag{2.2}$$

The choice of the neutral reference point in Figure 4, V_n, is arbitrary and only affects the zero sequence voltage (V_0). For the case where V_a is connected to the p bus and V_b and V_c are connected to the n bus (p, n, n) in Figure 4 the qd0 voltages are [7]:

$$\begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix} = \frac{V_{dc}}{2}\mathbf{K}_s \begin{bmatrix} 1 \\ -1 \\ -1 \end{bmatrix} = \begin{bmatrix} \frac{2V_{dc}}{3} \\ 0 \\ \frac{-V_{dc}}{6} \end{bmatrix} \tag{2.3}$$

Equation 2.3 also defines the length of the radii forming the corners of the hexagon, 2/3 V_{dc}. In the case where V_a and V_b are connected to the p bus and V_c is connected to the n bus (p,p,n) in Figure 4 the qd0 voltages are [7]:

$$\begin{bmatrix} v_q \\ v_d \\ v_0 \end{bmatrix} = \frac{V_{dc}}{2}\mathbf{K}_s \begin{bmatrix} 1 \\ 1 \\ -1 \end{bmatrix} = \begin{bmatrix} \frac{V_{dc}}{3} \\ \frac{-V_{dc}}{\sqrt{3}} \\ \frac{V_{dc}}{6} \end{bmatrix} \tag{2.4}$$

The two states defined by Equations 2.3 and 2.4 form the sides of Sector I. When the reference voltage is in this sector then these two states and the zero states are used to produce an output voltage that, in the average, equals the reference voltage. Let T_s be the total switching period, for example 100 μs when the switching frequency is 10 kHz. Let T_1 and T_2 represent the amount of time spent on states (p, n, n) and (p, p, n) respectively. The vectors V_1 and V_2 are proportional to the time spent on each state [7]:

$$V_1 = \frac{T_1}{T_s}\frac{2 \cdot V_{dc}}{3} \tag{2.5a}$$

$$V_2 = \frac{T_2}{T_s}\frac{2 \cdot V_{dc}}{3} \tag{2.5b}$$

The law of sines can be used to find the duty cycles for each state [7]:

$$\frac{2 \cdot V^*}{\sqrt{3}} = \frac{V_1}{\sin(60^o - \theta)} = \frac{V_2}{\sin(\theta)} \tag{2.6}$$

Substituting Equations 2.5a and 2.5b into Equation 2.6 yields solutions for the time spent on each state [7]:

$$T_1 = \frac{V^*\sqrt{3}}{V_{dc}} \cdot T_s \cdot \sin(60^o - \theta) \tag{2.7}$$

$$T_2 = \frac{V^*\sqrt{3}}{V_{dc}} \cdot T_s \cdot \sin(\theta) \tag{2.8}$$

The time spent on each state cannot exceed the total switching period so the modulation index is between zero and one [7]:

$$mi = \frac{V^*\sqrt{3}}{V_{dc}}, \quad 0 < mi < 1, \quad 0 < V^* < \frac{V_{dc}}{\sqrt{3}} \tag{2.9}$$

The amount of time spent in the zero state is the time remaining in the period [7]:

$$T_0 = T_s - T_1 - T_2 \tag{2.10}$$

The FPGA implementation presented here accomplishes the pattern shown in Figure 6.

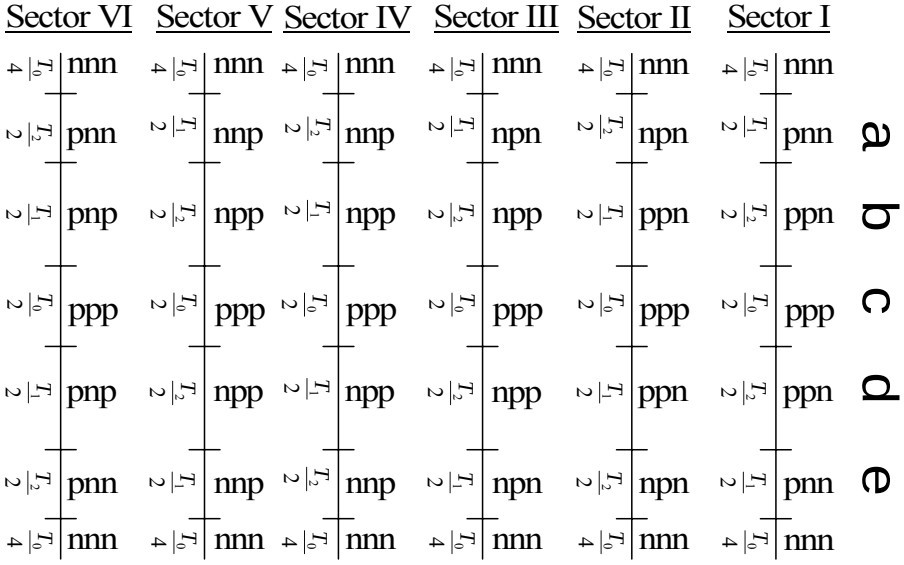

Figure 6. Switching Pattern From [7].

The space vector algorithm is shown in Figure 7 and was derived and mathematically modeled in MATLAB® using XILINX® products [7].

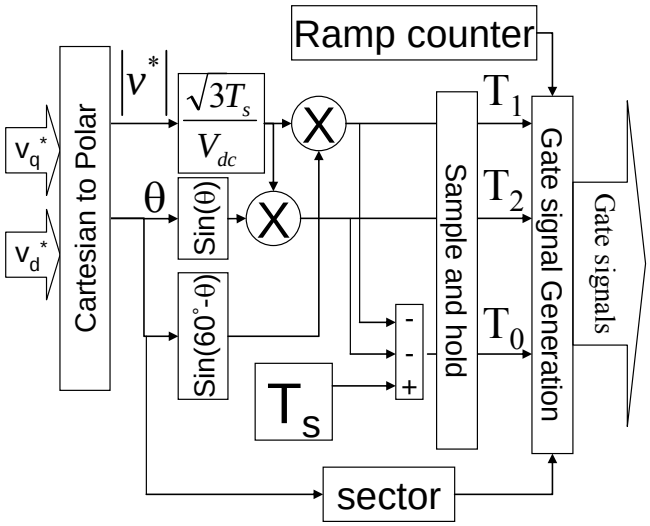

Figure 7. Space Vector Algorithm From [7].

The gate signal generator is shown in Figure 8. This produces the transistor gate signals that will be modified to correct the blanking time distortion.

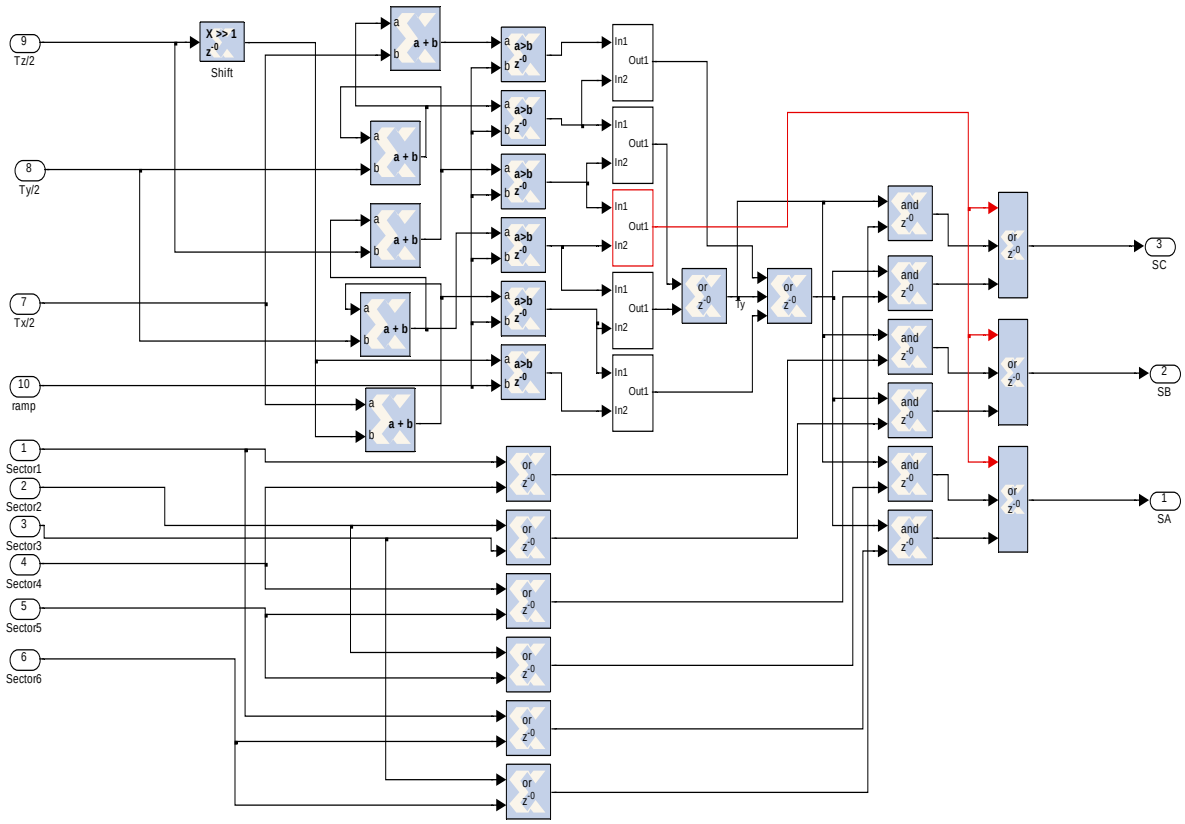

Figure 8. Gate Signal Drive Block.

C. BLANKING TIME DISTORTION

This thesis explores a method to compensate for the output voltage distortion in voltage source inverters (VSI) caused by the turn on delay inserted in a single phase inverter leg. When two transistors are connected in series across a capacitor source as shown in Figure 9, then they cannot both be on at the same time or a short circuit will occur. When one transistor is turned off, a delay is added before turning on the complementary transistor. This ensures a short circuit will not occur. This is referred to as blanking time and leads to unwanted output voltage distortion. A single leg of a VSI is illustrated in Figure 9.

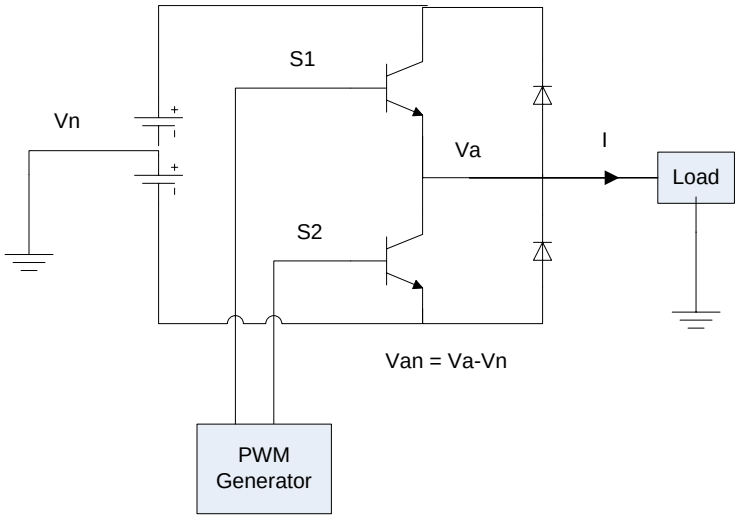

Figure 9. Single Voltage Source Inverter Leg.

In an ideal voltage source inverter the switching of individual legs is assumed to be perfect, which allows the state of the two transistors in an inverter leg to change simultaneously (when one turns off the other turns on). The bottom transistor is on when the top transistor is off and vice versa. Simultaneous switching is not possible in actual devices. There is a finite turn-off and turn-on time associated with any transistor. If both transistors in an inverter leg were on at the same time a short circuit would occur. Referring to Figure 9, if S1 is on then the turn on of the second transistor, S2, is delayed until the first has transitioned off and the blanking time has passed. This delay, often referred to as blanking time or dead time, is inserted to protect the device. The goal of this research is to compensate for the output voltage distortion caused by blanking time.

The blanking time t_Δ depends on how fast the transistor turns on and off. The dead time of common IGBT inverters used in industry vary between $t_\Delta \approx$ 1-5 μs [5]. The blanking time delay associated with the Semikron IGBT was measured at **3.8 μs**. This measurement was achieved by generating a specific gate signal to trigger the blanking time effect in the Semikron IGBT. The time delay between rising and falling edges of the known gate signal and the corresponding output pole voltage was measured. This procedure quantified the blanking time delay associated with the Semikron IGBT. The measurement was verified by the blanking time delay listed in the data sheet for the

IGBT Driver, included in Appendix B. The blanking time delay value was utilized to establish the time delay inserted in the simulation and compensation code.

D. BLANKING TIME COMPENSATION

In order to compensate for the blanking time delay a uniform delay is created. When the current polarity is positive the gate driver signal, s^*, is modified as shown in Figure 10. Turning off the transistor, S1, will immediately cause the output voltage to transition from $+V_{DC}/2$ to $-V_{DC}/2$ when the current is positive. Inserting a falling edge delay as shown in the modified gate signal in Figure 10 compensates for the blanking distortion when the current is positive.

When the current polarity is negative the rising edge of the ideal gate signal, s^*, is delayed as shown in Figure 10. The rising edge is delayed because when the current is flowing in the negative transistor S2 in Figure 9 and will turn off immediately if a delay is not added. If the ideal gate signal is used instead of the modified gate signal then the inverter output voltage will look like V_{AN} in Figure 10. Comparing V_{AN} (I>0 or I<0) and s^* in Figure 10 the difference in the waveform timing is the distortion that is to be eliminated. V_{AN} is different than s^*_{del} also. After compensation is added V_{AN} will have the same timing as s^*_{del}.

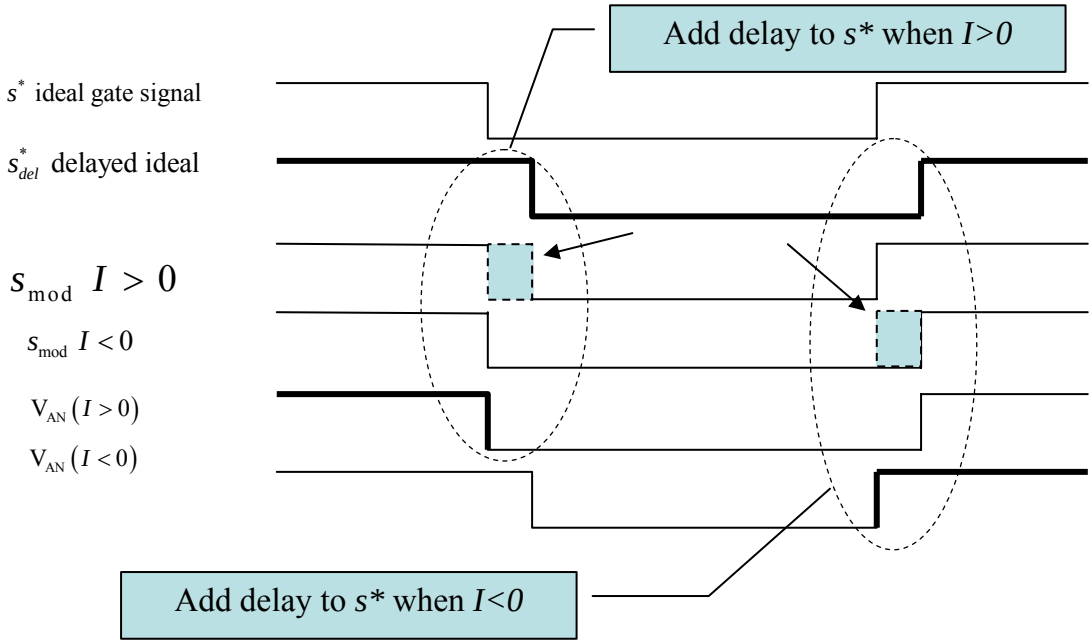

Figure 10. PWM signals with and without blanking time.

Referring to Figure 11, uniform delay is created and the compensated output voltage signals, V_{AN} (I>0) and V_{AN} (I<0) follow the delayed ideal signal, s^*_{del}. The blanking time correction is added to the ideal gate signal to create the fifth waveform in Figure 11, s_{mod} when the current is positive. A correction delay is added to the rising edge of s^* when the current is negative. The output voltage produced by the inverter V_{AN} (I>0) and V_{AN} (I<0) will be as shown in Figure 11 after the blanking time is reintroduced by the gate driver circuit.

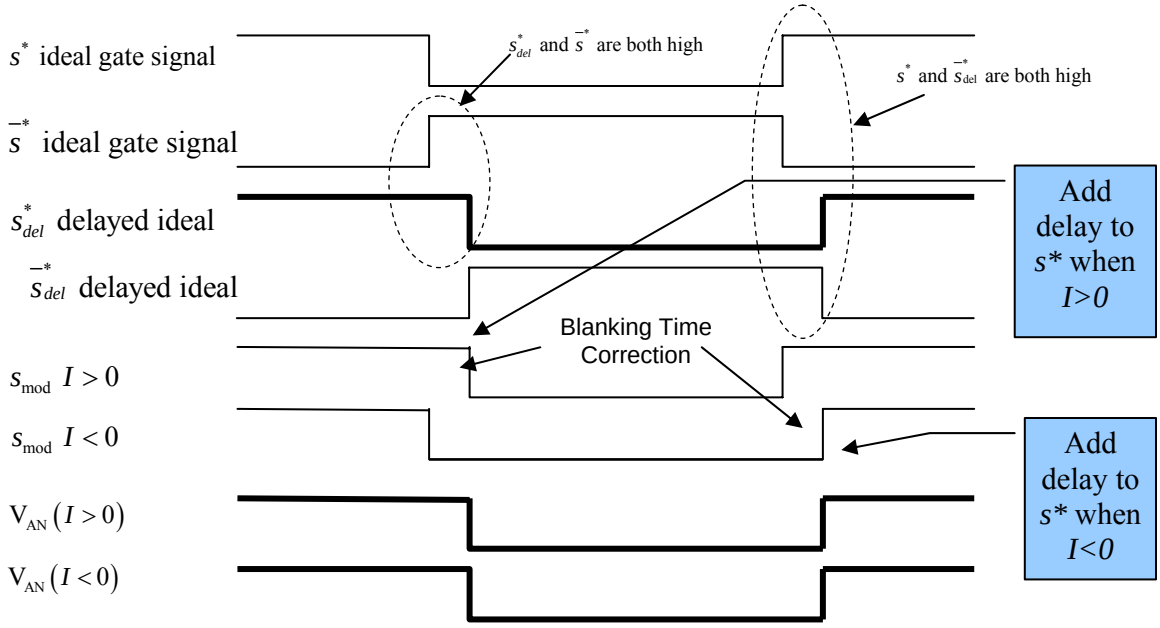

Figure 11. Compensated PWM Signals.

The modified gate signal causes the output voltage shape to be identical to the delayed ideal gate signal. This method creates uniform delay between the gate signal and the output voltage whether the current is positive or negative. This process compensates the blanking time delay.

E. XILINX® DESIGN IMPLEMENTATION

The design was implemented using the XILINX® blocks in Figure 12. Signal flow begins with the decision to enter the "iphase_pos" or "iphase_neg" block. This decision is based on the polarity of the phase current. The polarity of the current is converted into a Boolean value. A simple logic gate performs the conversion, if the value

of the current is greater than zero a one is produced by the logic gate. Conversely if the value of the current is less than zero a zero is generated. The current polarity is then used by the blanking time correction software. If the current is positive the MUX will select d1 as the value of iphase as one and the output from the upper block iphase_pos in Figure 12 will be selected. If the current is negative the value of iphase is zero and the output from the lower box iphase_neg, Figure 12 is chosen.

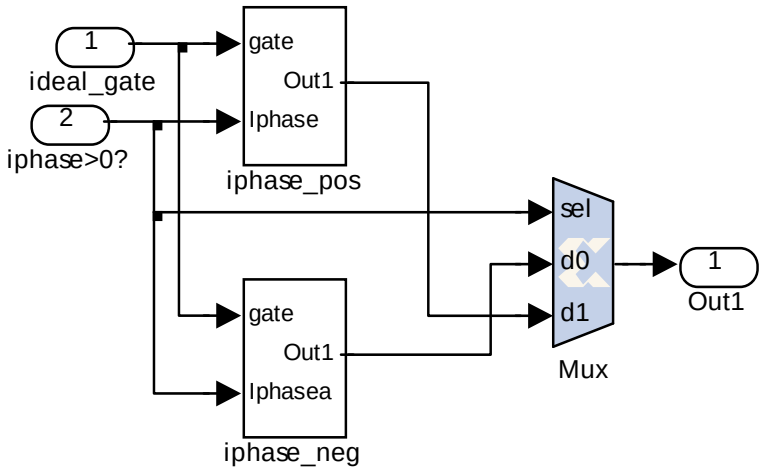

Figure 12. Blanking Compensation.

If the current polarity is positive the MUX will choose d1 and output iphase_pos. The iphase_pos block of the model is shown in Figure 13. The intent is to delay the falling edge of the gate signal.

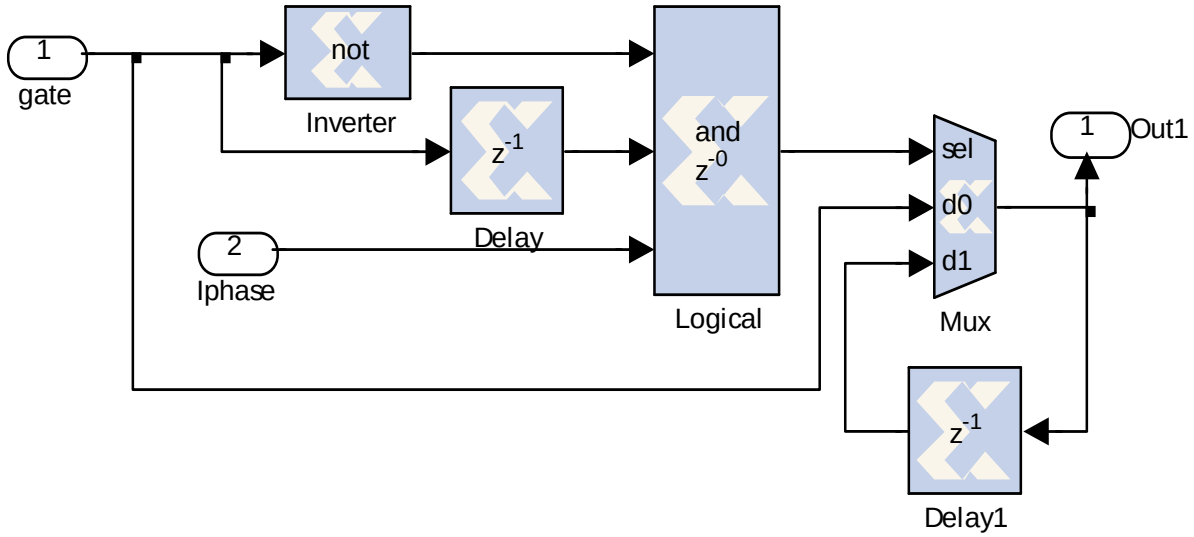

Figure 13. IPhase_Pos Compensator Block Model.

The logical AND block in Figure 13 only provides a boolean value of one if all three input conditions are met:

- The polarity of the current is positive
- The inverse value of the gate is high
- The delayed gate signal value is high (delay=3.8μs)

When sel=1 the d1 port on the MUX is chosen and the value of the output at the last clock cycle is sent as the output gate signal. This process continues, delaying the falling edge of the gate signal for 3.8 microseconds until the delay is over and the delayed gate signal value drops to zero producing a boolean 0 at the AND input. The AND logic now produces a 0 and the d0 port of the MUX is chosen. This outputs the normal gate signal.

Figure 14 shows the iphase_neg block which is selected when the current polarity is negative. When the polarity of the current is negative the intent is to delay the rising edge of the gate signal.

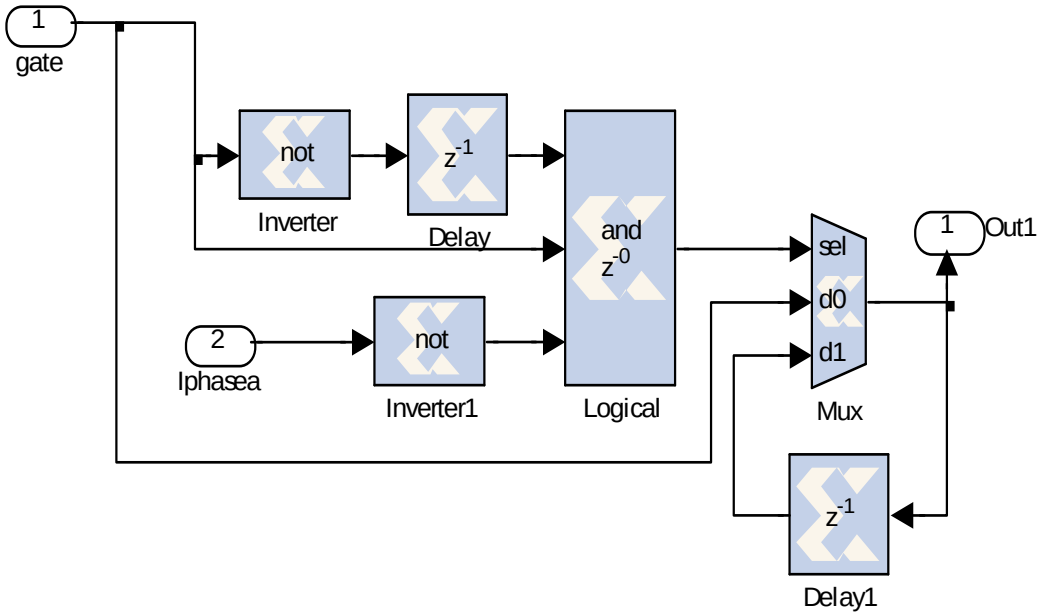

Figure 14. IPhase_Neg Compensator Block Model.

The logical AND block only provides a boolean value of one if all three input conditions are met:

- The polarity of the current is negative
- The gate signal has transitioned to high
- The inverse of the delayed input gate signal is high (delay=3.8μs)

The d1 port on the MUX is chosen and the value of the output at the last clock cycle is sent as the output gate signal. This process delays the rising edge of the gate signal for 3.8 microseconds until the delay is over and the inverted delayed gate signal value changes to zero producing a Boolean 0 at the AND input. The AND logic now produces a 0 and the d0 port of the MUX is chosen which outputs the normal gate signal, which is high, as it has been for the duration of the delay.

F. SUMMARY

This chapter presented the heart of this research, the blanking time compensation approach. The chapter also explained the method, implementation, and design of the compensator. The next chapter describes the computer modeling and simulation.

III. COMPUTER MODELING AND SIMULATION

A. OVERVIEW

This chapter describes the computer modeling and simulation results. The components are modeled mathematically using SIMULINK®. The model predicts the VSI output voltage distortion with and without blanking compensation. The entire model is included in Appendix A.

B. SIMULATION MODEL

The simulation is a simplified version of the overall system model presented in Section II. The space vector modulation is the same as provided in [7]. The PWM control gate signals are driven through a simulated load after the distortion caused by blanking time and forward voltage drop has been added. The model predicts the output voltage waveform, and is similar to the experimental results. The experimental results are presented in a follow-on chapter. Figure 15 shows the simulated load that is driven by the previous simulation model. The individual model blocks are described in more detail in the following sections.

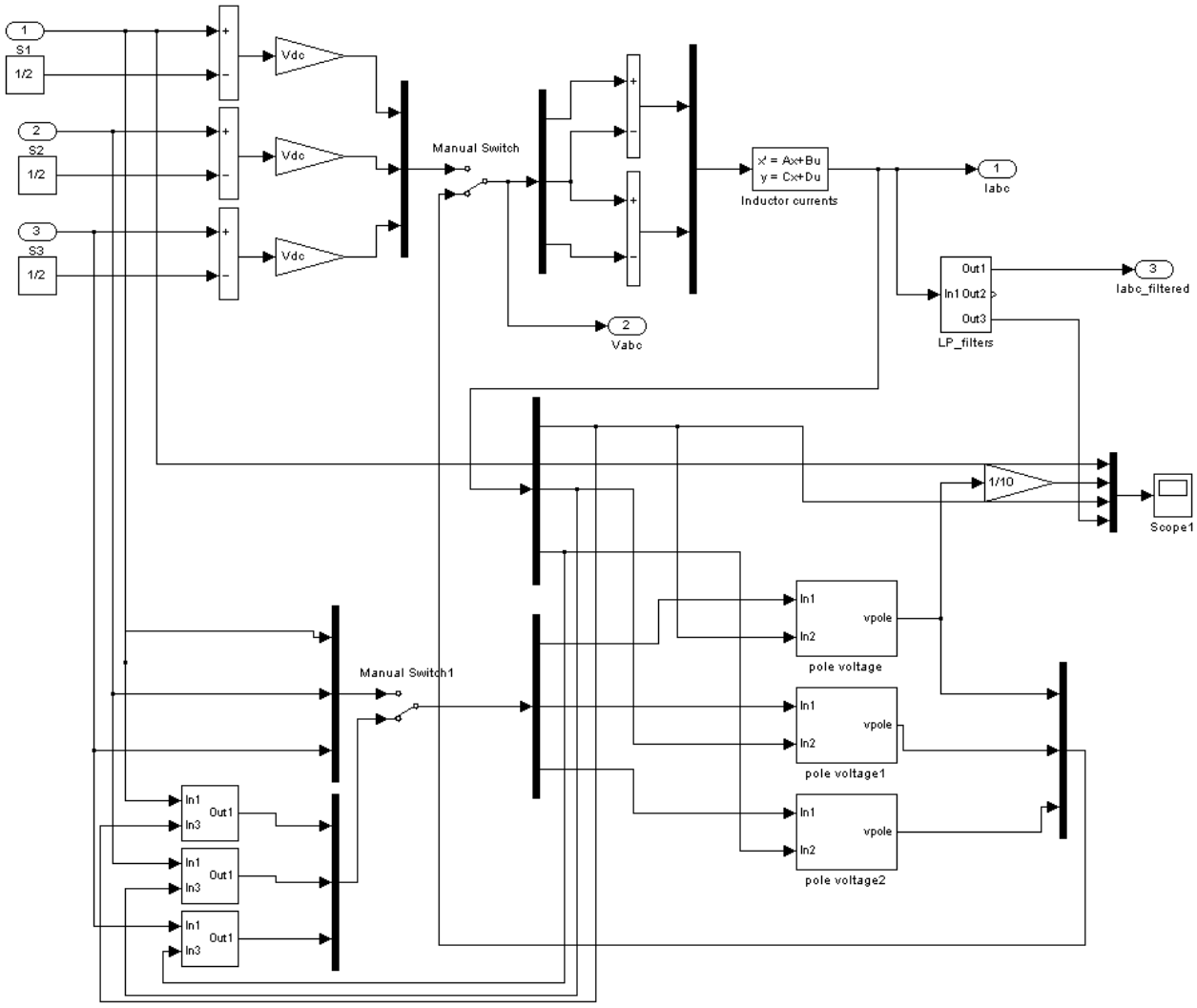

Figure 15. Filter and RL Load Model Block.

This simulation contains two manual switches which allow multiple scenarios to be run from the same model. The upper switch in Figure 15 controls whether or not the ideal system is simulated. This represents the baseline or best case output voltage. When the upper switch is toggled to the secondary position the blanking time and forward voltage drop distortions are added. The simulation now represents how the real world inverter behaves. The lower switch either inserts the blanking time compensation code or removes it from the simulation. These manual switches allow the output voltage to be recorded in the ideal case, non-ideal case, and with the blanking time compensation code inserted.

C. BLANKING TIME DISTORTION MODEL BLOCK

The XILINX® block in Figure 16 inserts the blanking time delay into the system model to replicate the real world Semikron SemiTeach IGBT. The code adds a 3.8μs delay to the gate signal to duplicate the blanking time delay implemented in the IGBT gate drive to prevent instantaneous switching and cross conduction current.

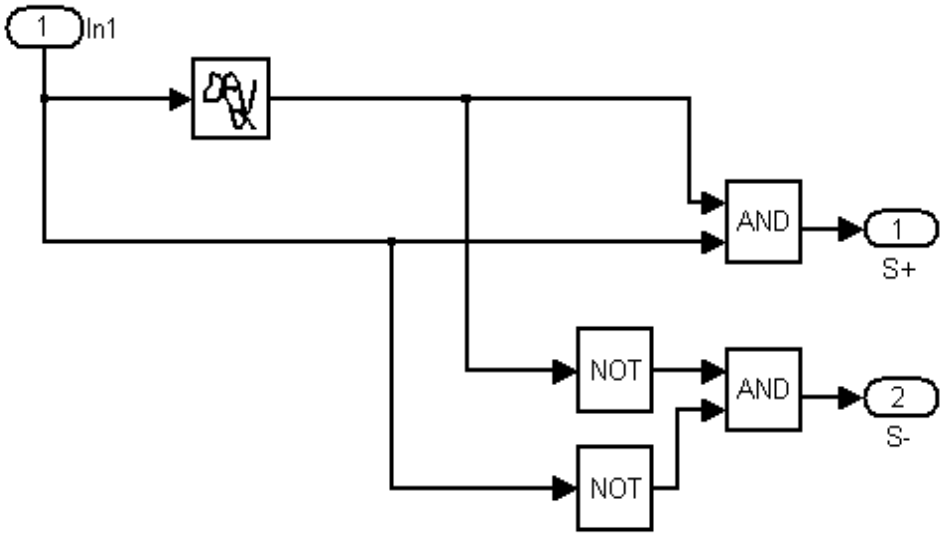

Figure 16. Simulated Blanking Time Block.

D. FORWARD VOLTAGE DROP MODEL BLOCK

The forward voltage drop in the IGBT is modeled by the block shown in Figure 17. The block utilizes a lookup table to determine which voltage is added to the DC bus input to represent the voltage drop of the switching device.

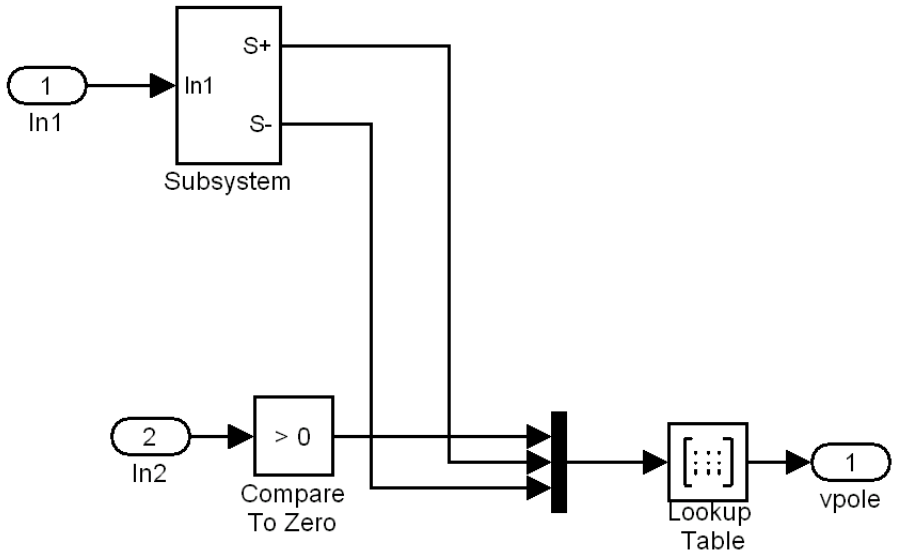

Figure 17. Simulated Forward Voltage Drop Block.

The software lookup table for the voltage drop block is shown in Table 1. The corresponding output is based on the input received into the multiplexer and represents the actual output pole voltage.

I > 0	**S^+**	**S^-**	**V_o**
0	0	0	$V_{dcp} + V_d$
0	0	1	$V_{dcn} + V_{CEsat}$
0	1	0	$V_{dcp} + V_d$
0	1	1	0
1	0	0	$V_{dcp} - V_d$
1	0	1	$V_{dcp} - V_d$
1	1	0	$V_{dcn} - V_{CEsat}$
1	1	1	0

Table 1. Software Lookup Table.

E. SIMULATION RESULTS

The simulations are run with 90 VDC and a three phase balanced load. The model performs as expected. There is significant distortion in the output voltage spectrum when the known distortion sources are added (Figure 19) compared to the ideal case (Figure 18). The voltage spectrum shown in Figure 20 demonstrates the improvements expected when the blanking time compensation block is added to the simulation. The blanking time correction code improves the output voltage and reduces the fifth harmonic. The output voltage for the ideal simulation is shown in Figure 18.

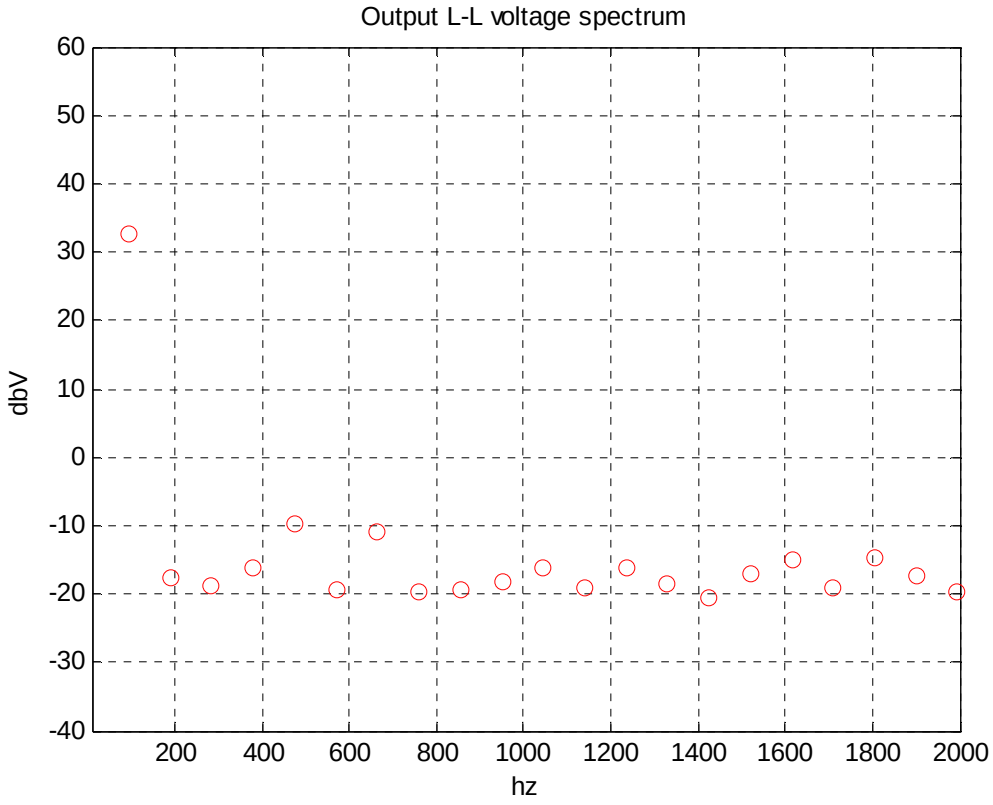

Figure 18. Ideal Simulated Output Spectrum.

The calculated THD for this simulation was **-47.9dB.**

The simulated line to line output voltage spectrum with forward voltage drop and blanking time distortions added is shown in Figure 19.

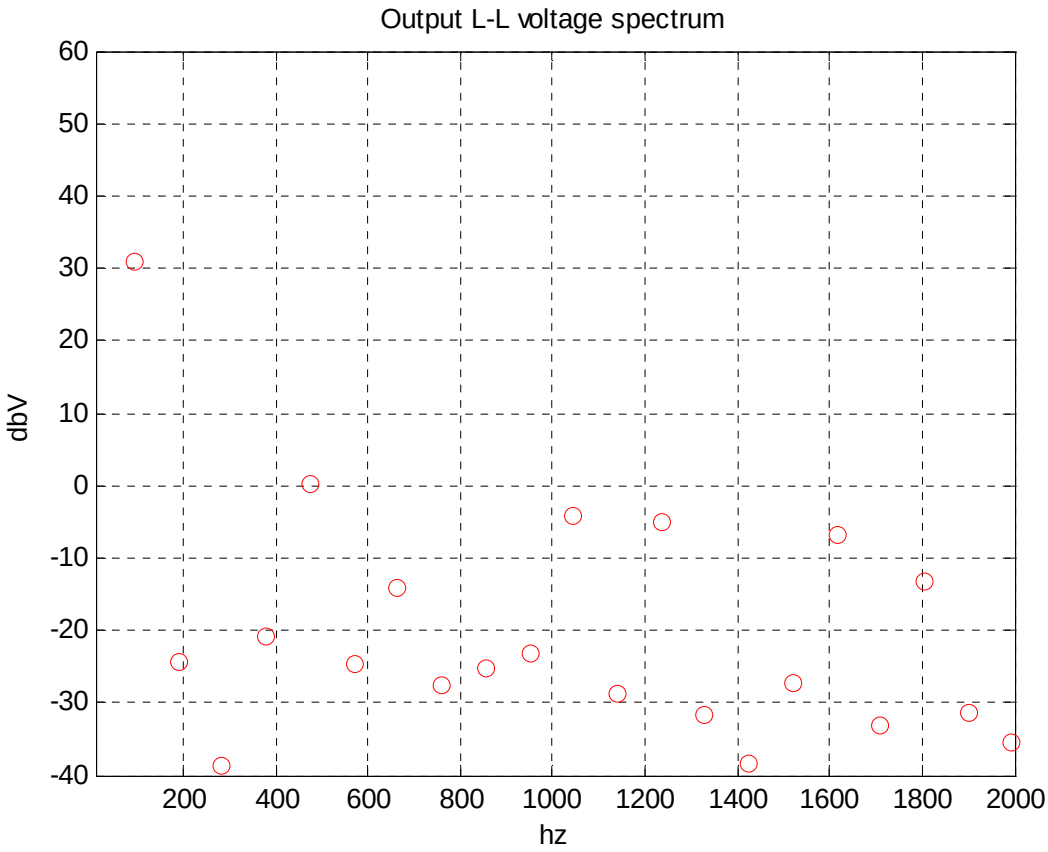

Figure 19. Simulated output with Forward voltage drop and blanking time distortions inserted.

The THD for Figure 19 was **-27.65dB**, and demonstrates the voltage distortion associated with the blanking time delay and the forward voltage drop of the switching devices. The fifth harmonic is much larger than Figure 18.

The simulated line to line output voltage spectrum with forward voltage drop, blanking time distortion and the blanking time compensation block is shown in Figure 20.

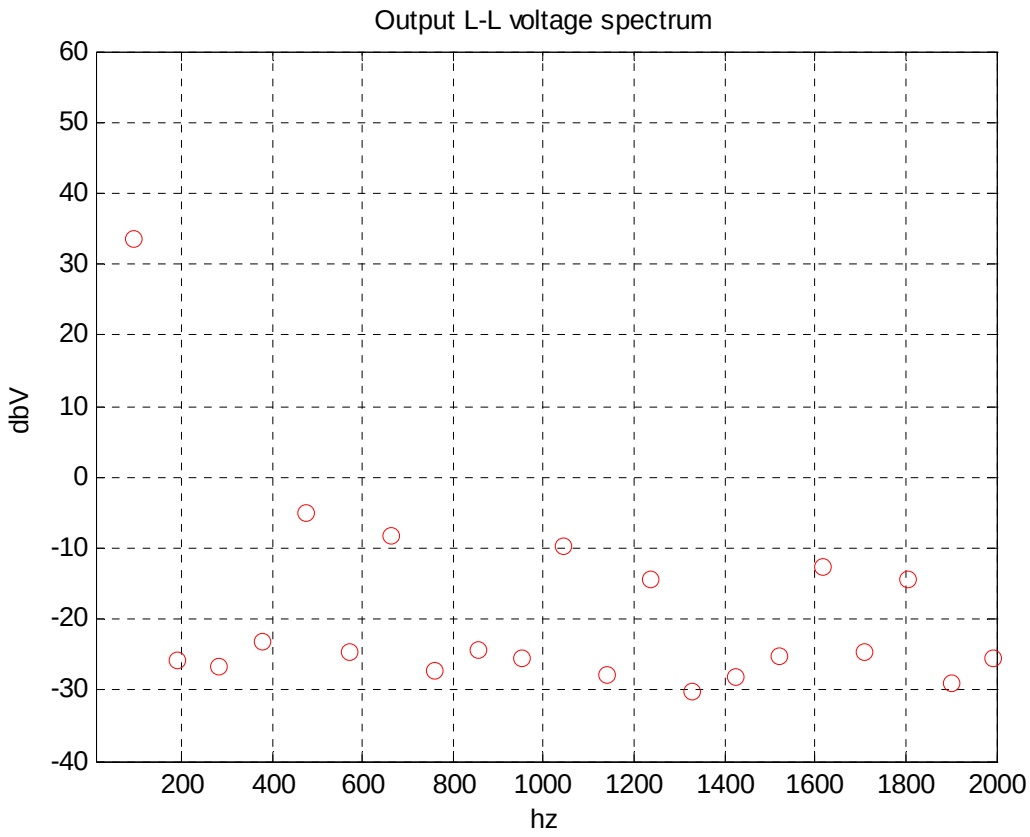

Figure 20. Simulated output with Forward voltage drop and blanking time inserted with compensation code.

The THD in Figure 20 is **-31.1dB,** which is a significant improvement from the THD from Figure 19 (**-27.65dB**). The results of the simulation predict considerable improvement in the output voltage spectrum when the compensation is added.

F. SUMMARY

This chapter provided simulated predictions of the effectiveness of the blanking time compensator code. The next chapter will provide an overview of the major components utilized to test the compensation method in the laboratory through experimentation.

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IV. HARDWARE CONFIGURATION

A. OVERVIEW

The primary hardware utilized in this thesis consisted of the Virtex II™ development kit which contains the Virtex II™ FPGA, the Semikron SemiTeach IGBT, the NPS Interface board, and a three-phase wye connected load. The wye connected three phase load consisted of a 58Ω resistor and a 2.12 mH inductor. Each component and setup is described in this chapter.

B. FIELD PROGRAMMABLE GATE ARRAY

An FPGA is a generic semiconductor device containing a large number of programmable logic components and interconnects. The logic components can be programmed to duplicate the functionality of basic gates such as AND, OR, XOR, and NOT. FPGAs are also capable of performing simple math functions. The FPGA can be traced back to Complex Programmable Logic Devices (CPLD) of the early 1980s. The CPLDs were only able to contain several thousand logic gates, while the FPGA can contain over a million [9]. The FPGA utilized in this research is the XILINX® XC2V1000-4FG256C FPGA, contained the in Virtex II™ development kit shown in Figure 21. The default clock runs at 100MHz. The 5.0V connector pin is used to supply the main power to the card. All other card power is derived from this 5.0V input. The specification sheet is included in Appendix A.

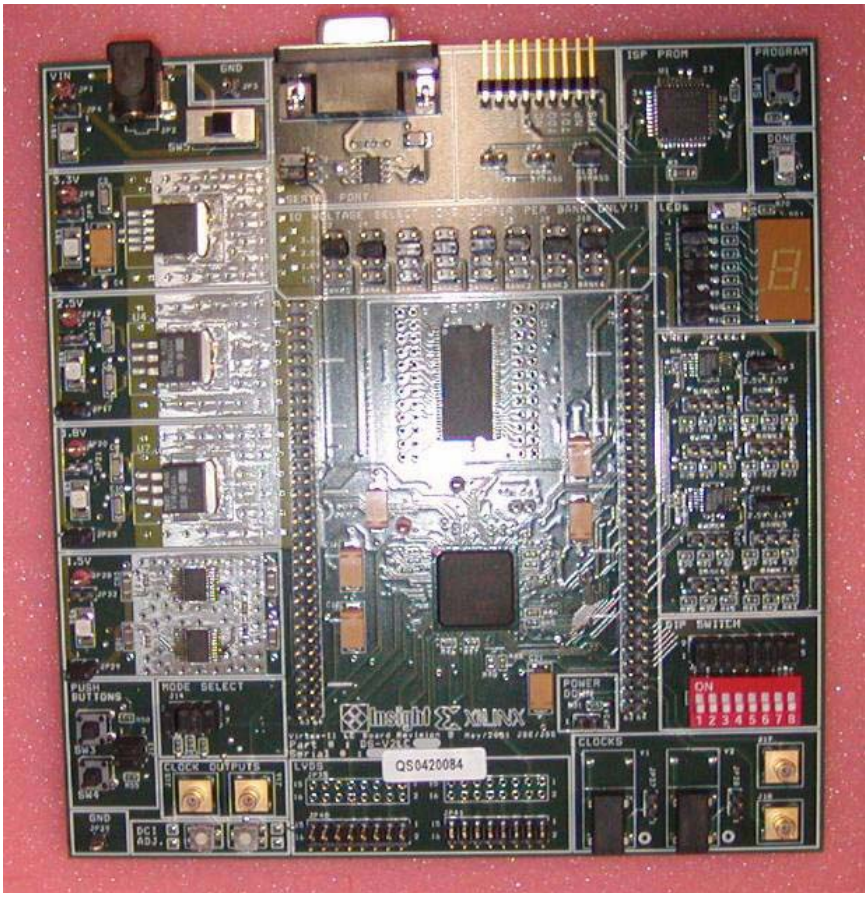


Figure 21. Virtex II™ Development Kit From [9].

The FPGA allows the Pulse-width modulation scheme presented in this thesis to be implemented. The scheme requires double sampling per carrier period which may not have been feasible had a Digital Signal Processor been used to implement the design. The block diagram for the Virtex II™ is shown in Figure 22. SIMULINK® inside MATLAB® was used to generate the programming code based on the block diagrams.

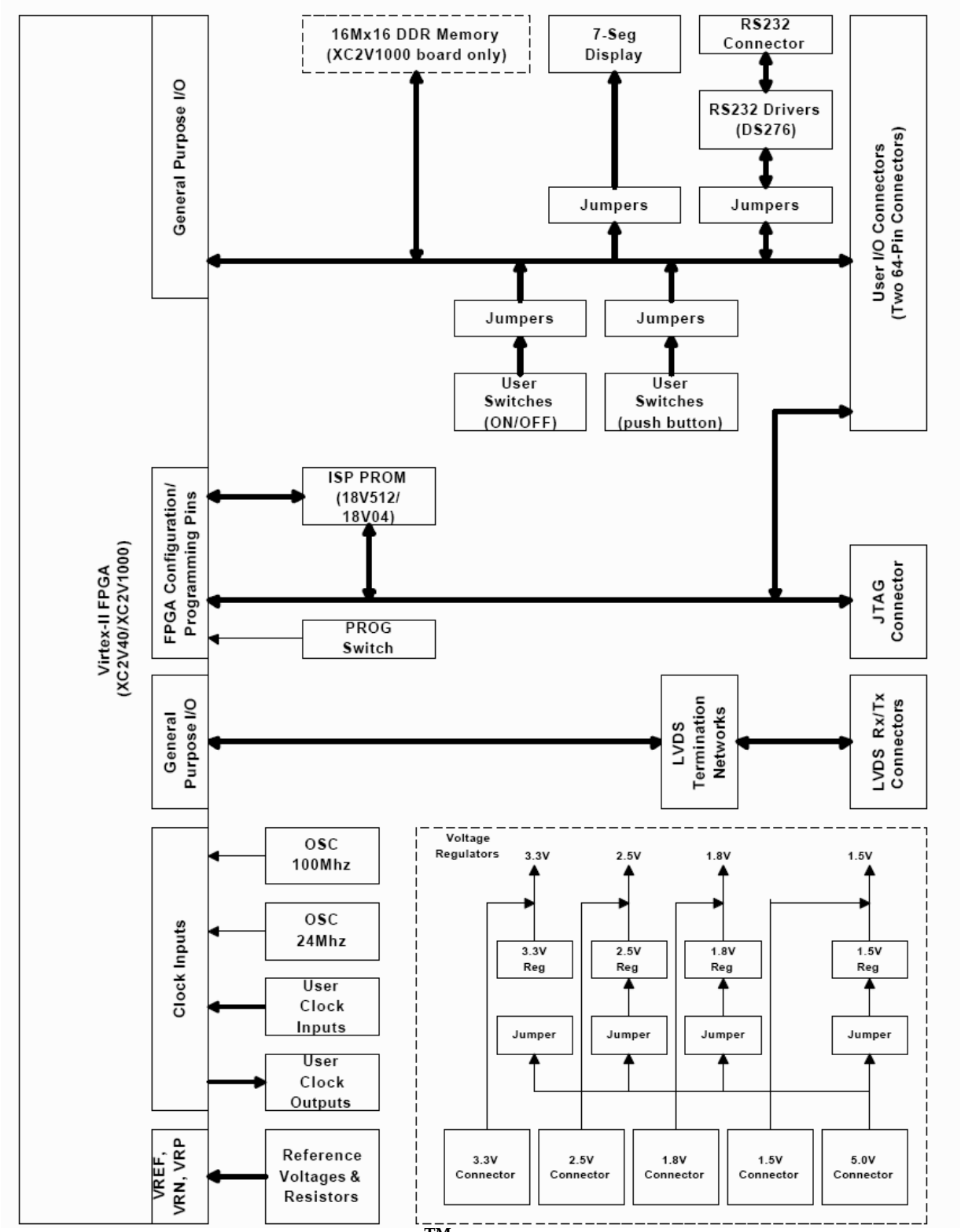


Figure 22. Virtex II™ Block Diagram From [9].

C. VOLTAGE-SOURCE INVERTER

A six-step controlled VSI is the output power device used in these experiments. The Semikron SemiTeach VSI has three half-bridge modules consisting of two IGBTs with freewheeling diodes as shown in Figure 23 (*S1*-*S2*, *S3*-*S4* and *S5*-*S6*). Each half-bridge is integrated as a SKM 50 GB 123 D module.

> The gate driver that controls both IGBTs in each half-bridge is a SKHI 22B. This commercial driver offers the following built-in features: It provides galvanic isolation between the high voltage section and the controller card. It prevents simultaneous gating of upper and lower switches. It has short-pulse suppression where a gating pulse must be >500ns. It provides under voltage protection. It provides short-circuit protection through the monitoring of collector-to-emitter voltage [9].

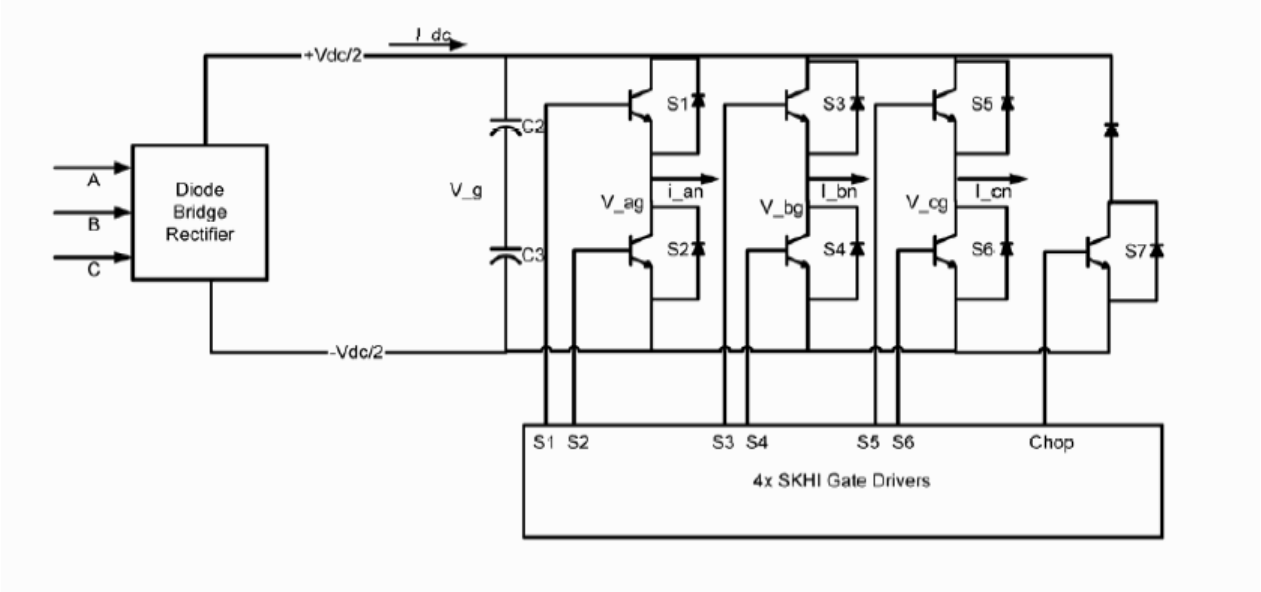


Figure 23. Semikron SemiTeach Schematic From [9].

The inverter is contained in Plexiglas to allow students to see its interworkings and to identify parts. The entire apparatus is shown in Figure 24.

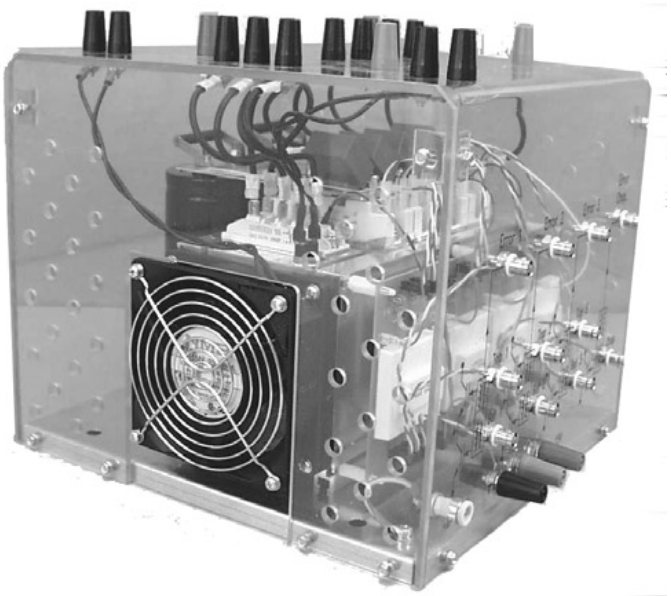


Figure 24. Semikron SemiTeach IGBT.

D. INTERFACE BOARD

An interface was required to connect the FPGA to the Semikron IGBT; this required a user designed interface board with BNC connectors to transmit the PWM signals from the FPGA to the Semikron IGBT.

The interface card performs the following functions:

- It supplies 5V power to the Virtex II™ development kit.
- It level shifts the low voltage gate driver signals from the development kit
- It contains an interface to the development kit.
- It provides 12 BNC connectors for the gate signals to the Semikron IGBT.
- It provides test points for troubleshooting.

After outlining these required functions, components were identified for individual need. The interface card was designed using a software package that allows quick design implementation of multi-layer boards (PCB123®). The bottom of the card contains the Virtex II™ interface connectors and the top of the card contains the rest of the components and connectors [9].

The wiring schematic and printed circuit board are shown in Figure 25. Figure 26 is a display of the interface board fully connected to the Virtex II™ FPGA.

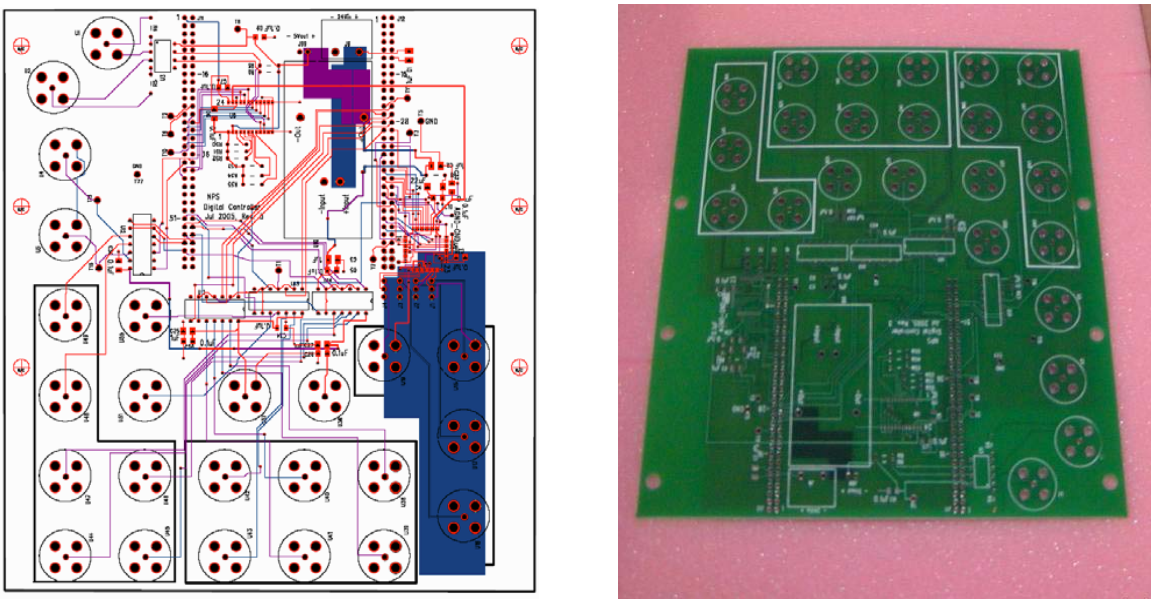


Figure 25. Interface Board From [9].

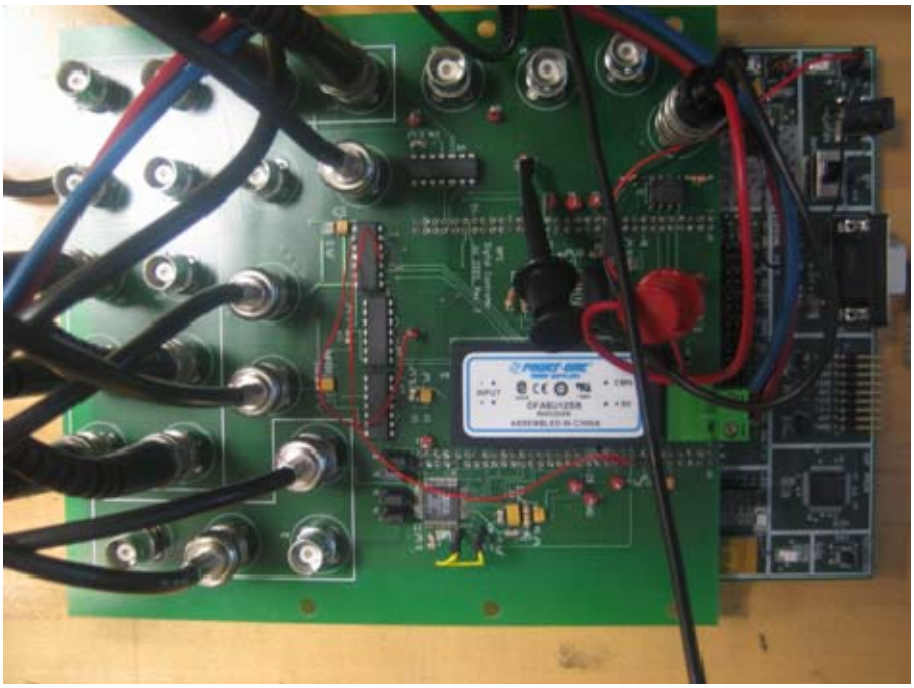


Figure 26. Connected Interface board.

E. LOAD

The load for the experiments conducted in the next chapter is very important. Its impact on the phase current is very important as that current is used to make the logical decision for the blanking time compensation code. The load consists of a three phase wye-connected 58Ω resistor and a 2.12 mH inductor as shown in Figure 27.

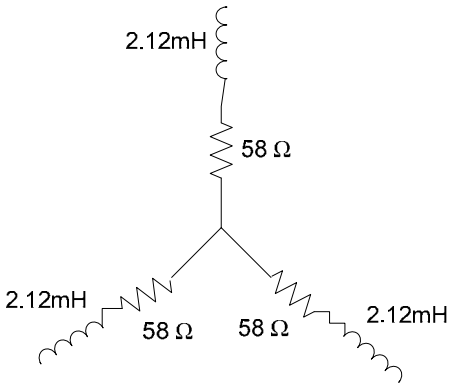


Figure 27. Three phase wye-connected load.

The physical components used had to be capable of handling high voltages so the INVERPOWER® Controls limited model P-108 RL resistive load was utilized. It rates 3KW-230 Volts. The inductors, also from INVERPOWER®, are rated for 10A MAX and tunable in the range of 42.5mH – 2.125mH. Figure 28 shows the physical load components.

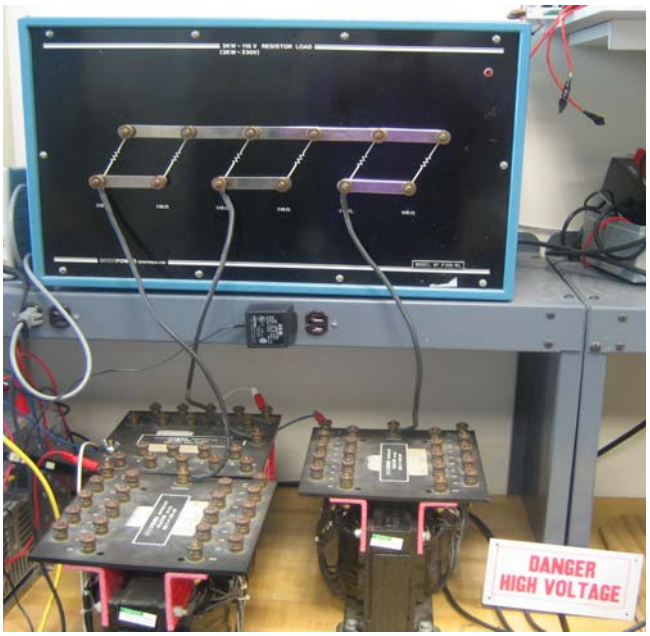


Figure 28. Load Components.

The three phase AC power supply shown in Figure 29 supplies the main power for the inverter. It produces a maximum 280V, 12.1 KVA at a max 25 amps and operates at 60Hz.

Figure 29. Three Phase AC Power Supply.

F. SUMMARY

This chapter provided an overview of the major components utilized to test the compensation approach presented in this thesis. The next chapter presents the laboratory results from the blanking time compensator tests.

V. LABORATORY TEST AND CONCEPT VALIDATION

A. OVERVIEW

The chapter presents the results from the testing of the blanking time compensation code when used to generate PWM control for the VSI. The applied voltage across the DC Bus was 90 volts. The voltage probe was set to 50:1 scale for the output voltage and the oscilloscope probe was set to 1X for all measurements.

B. COMPENSATION CODE TEST

The determination if the XILINX® design is correctly compensating for the blanking time delay is made by comparing the delay between the PWM gate signal generated by the FPGA to the output pole voltage of the corresponding phase. These measurements are taken in two different instances, first without the compensation code and then with the compensation code inserted.

Figure 30 and Figure 31 are two snapshots of the gate signal and the inverter pole voltage without compensation. The two scope plots show that the falling edge delay between the gate signal and the output voltage varies (2.69 μs in Figure 30 and 5.28 μs in Figure 31). These experiments show that the insertion of blanking time results in different time delays between the gate signal (blue) and the pole voltage (aqua).

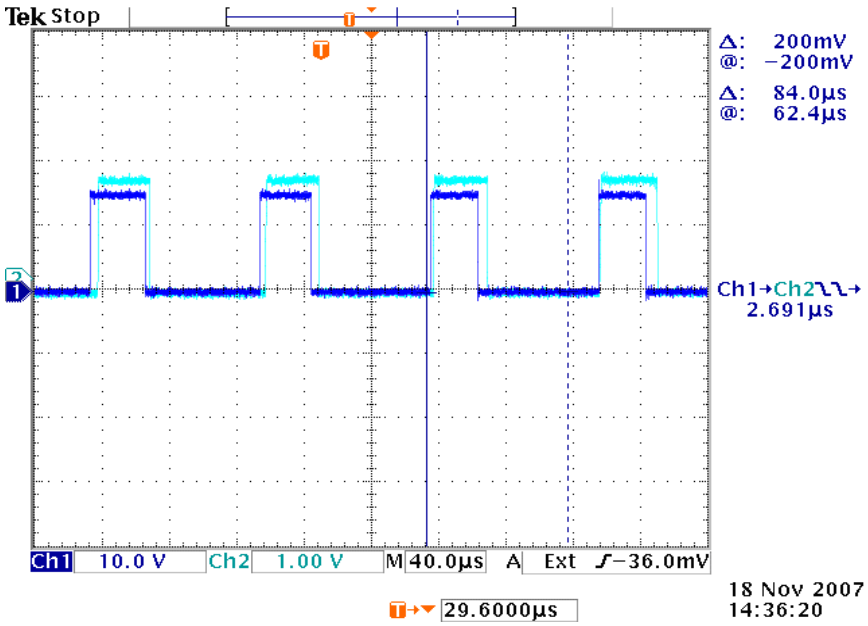


Figure 30. FPGA Gate Signal (blue) and Output voltage (aqua) falling edge delay.

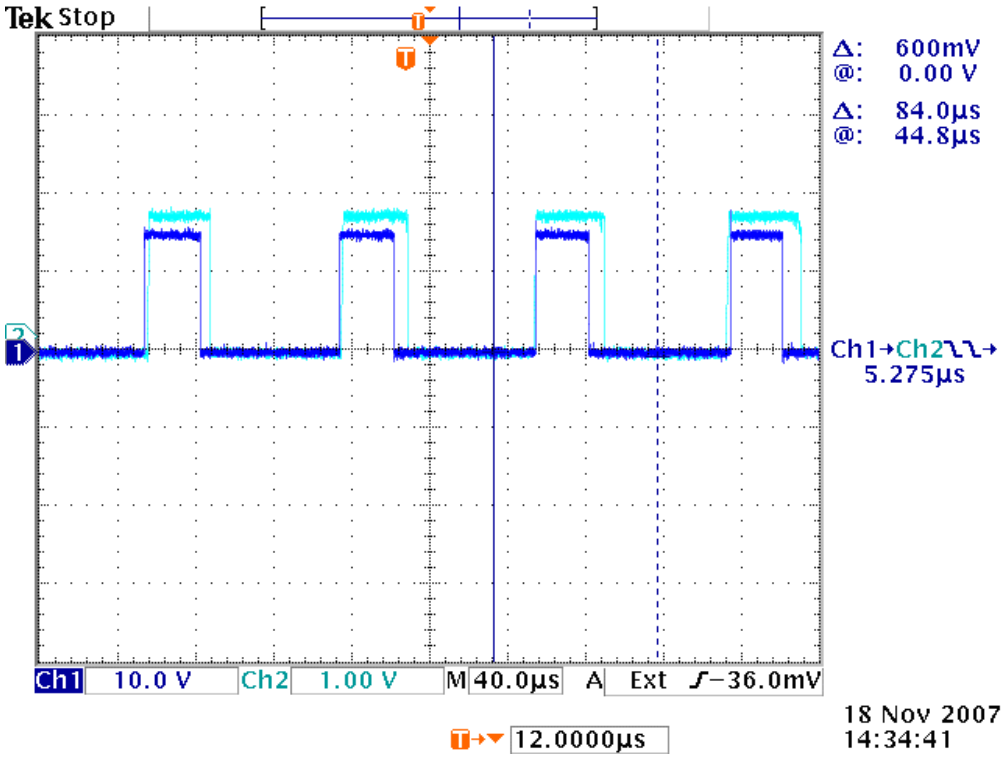


Figure 31. FPGA Gate Signal (blue) and Output voltage (aqua) falling edge delay.

The gate signal and output voltage delay dissimilarity can also be seen in Figures 32 and 33 where the rising edge of the output voltage is delayed (5.64 µs in Figure 32 and 2.95 µs in Figure 33).

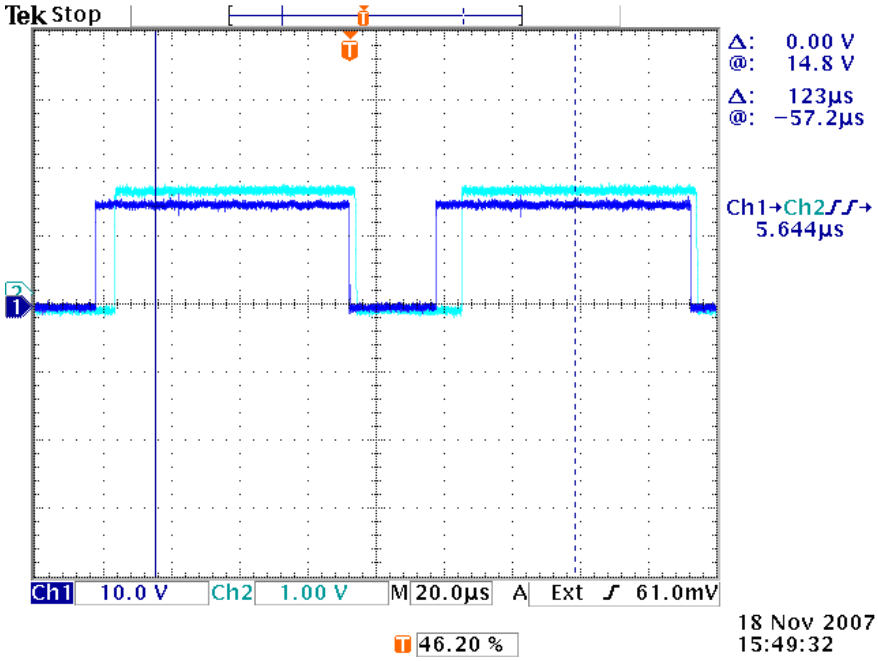


Figure 32. FPGA Gate Signal (blue) and Output voltage (aqua) rising edge delay.

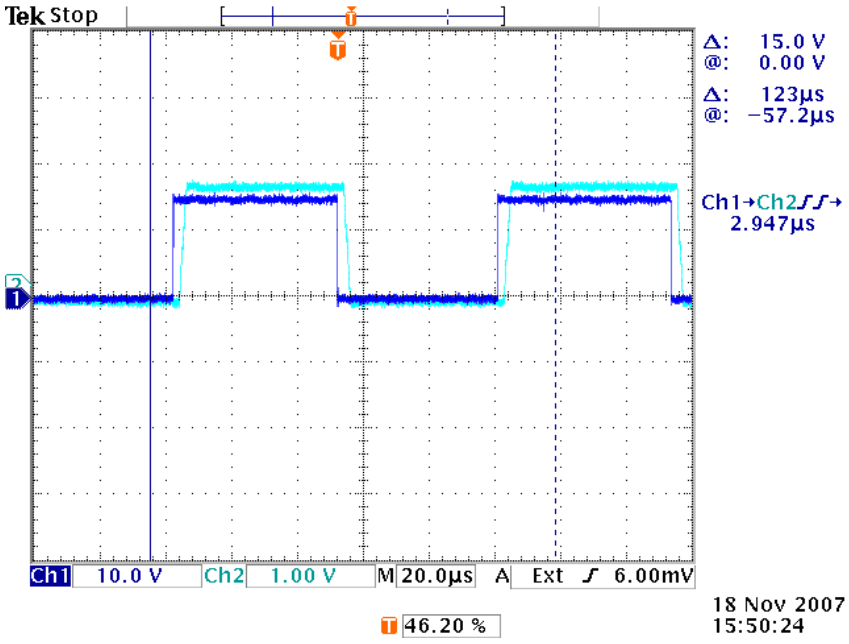


Figure 33. FPGA Gate Signal (blue) and Output voltage (aqua) rising edge delay.

Table 2 was compiled from several different random oscilloscope measurements and shows the difference in the delay time from the PWM signal generated by the FPGA and the phase voltage from the inverter as the current changes polarity. The variations are due to the insertion of blanking time and the current polarity as discussed in Chapter II.

Attempt	Channel 1(Gate Signal) to Channel 2(Pole Voltage) Delay in μs
1	5.595
2	5.461
3	2.688
4	5.437
5	2.692
6	2.654
7	5.673
8	5.575

Table 2. Switching Delay Times.

The phase A current, shown in Figure 34, was used as an external trigger to test the compensation method with positive and negative current. The trigger level was set a 250mA to obtain a snapshot of the delay between gate signal and the output pole voltage with positive current. Next, the trigger level was set to -250mA in order to obtain a snapshot of the same delay with negative current.

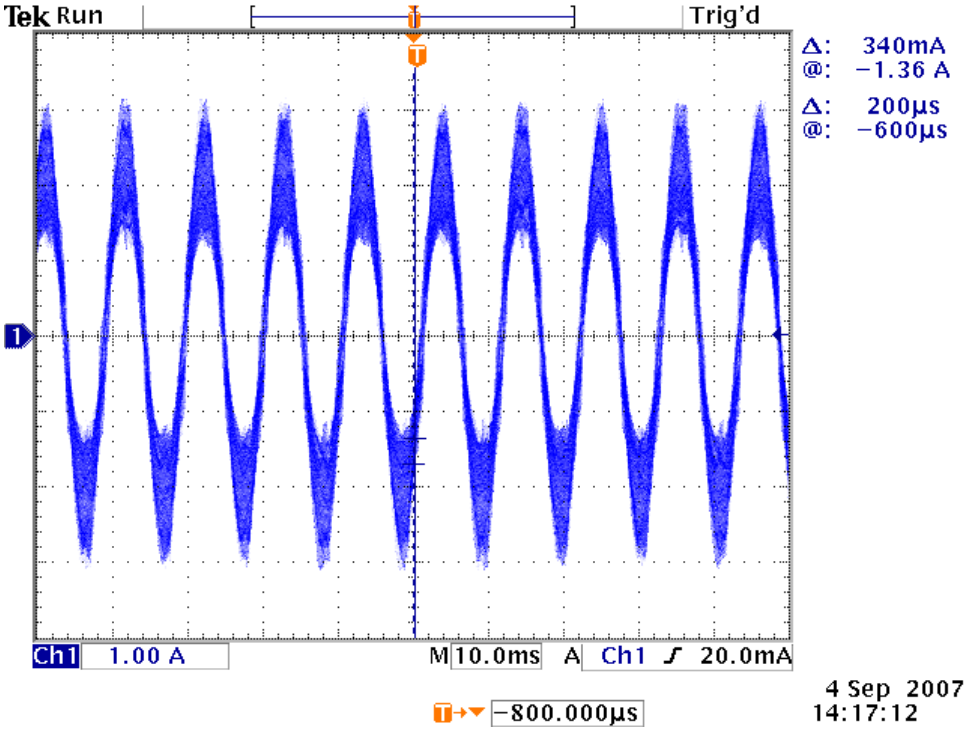


Figure 34. Phase A Current.

The oscilloscope image in Figure 35 was taken with the blanking time compensation code inserted and the delay between the PWM signal output from the FPGA and the corresponding phase voltage were consistency close to one another, roughly **5.6-5.8µs**. Figure 35 verifies that the blanking time compensation code works properly. The delay between the rising edge of the gate signal and the rising edge of the pole voltage is almost the identical to the delay between the falling edge of the gate signal and the pole voltage. This delay, with blanking time compensation, is independent of the polarity of the phase current. The compensation code successfully created a uniform delay between the gate signal and the pole voltage as described in Chapter II Figure 11.

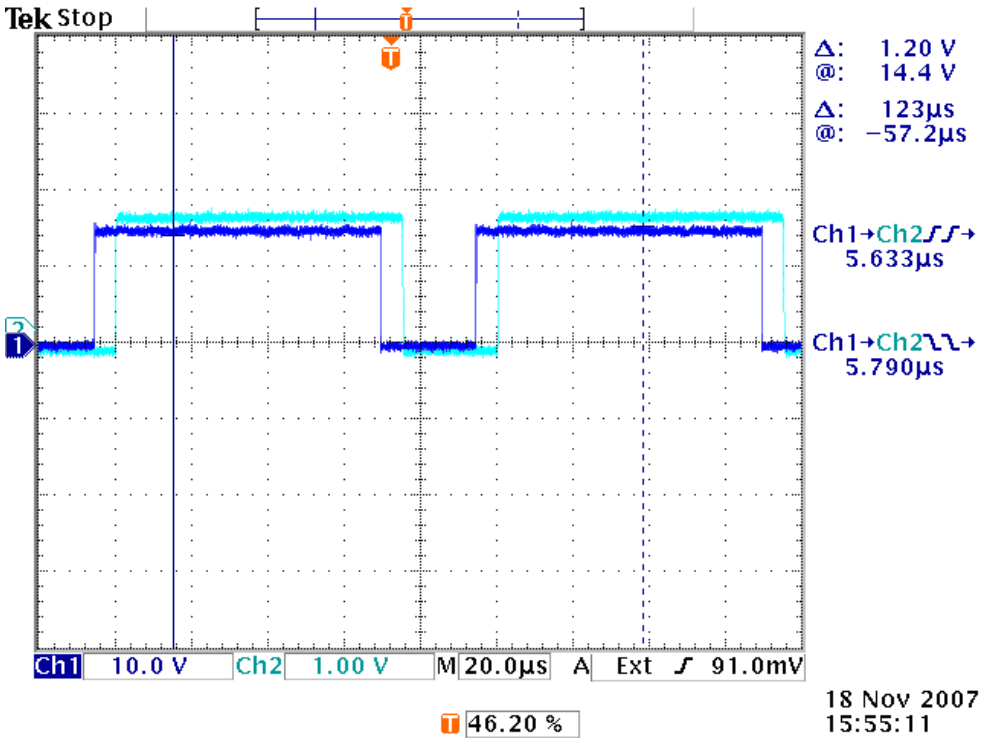


Figure 35. Uniform Delay between FPGA Gate Signals (blue) and Phase A output voltage (aqua).

Table 3 was compiled from several different random oscilloscope measurements and show the effectiveness of the blanking time compensator. The delay between the rising and failing edges of the PWM signal directly from the FPGA and the pole voltage are nearly uniform at every instance.

Attempt	Channel 1 to Channel 2 Delay in µs
1	5.592
2	5.587
3	5.598
4	5.601
5	5.591
6	5.588
7	5.594
8	5.592

Table 3. Switching delay.

C. SPECTRUM ANALYSIS

The results below quantify the effects of the pulse based compensation approach utilized in this thesis. All tests were run with 90 volts across the DC bus and the same three-phase load. The voltage probe was set to 50:1 scale.

1. No Blanking Time Compensation

Figure 36 shows the gate signal line to line spectrum observed without the blanking time compensation code inserted in the PWM signal. This is the baseline for testing the effectiveness of the blanking time code. This PWM signal output is fed directly into the Semikron SemiTeach IGBT and drives the inverter output. The THD measured by the spectrum analyzer was **-49.21dB**.

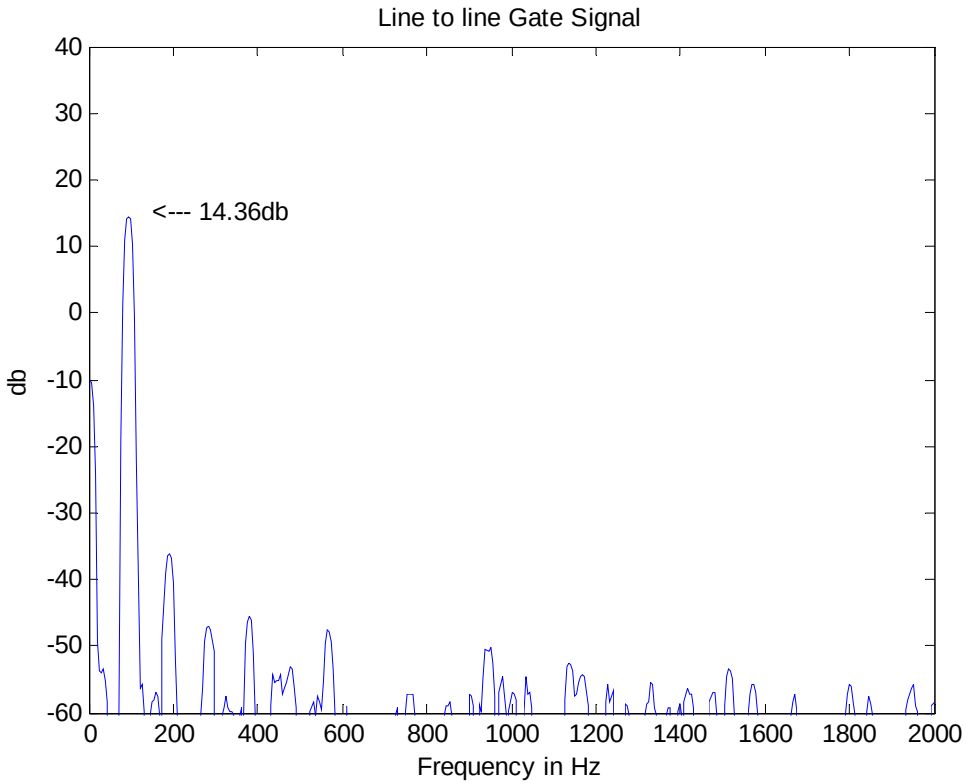


Figure 36. Gate signal Spectrum.

Figure 37 shows the line to line output of inverter poles A and B (V_{AB}). The measured THD for this output was **-35.72dB**. This is substantially lower than the "pure" signal generated by the FPGA in Figure 36. There are several factors that contribute to

the reduction in signal quality. This research effort makes an attempt to improve the output voltage spectrum by compensating for the blanking time distortion.

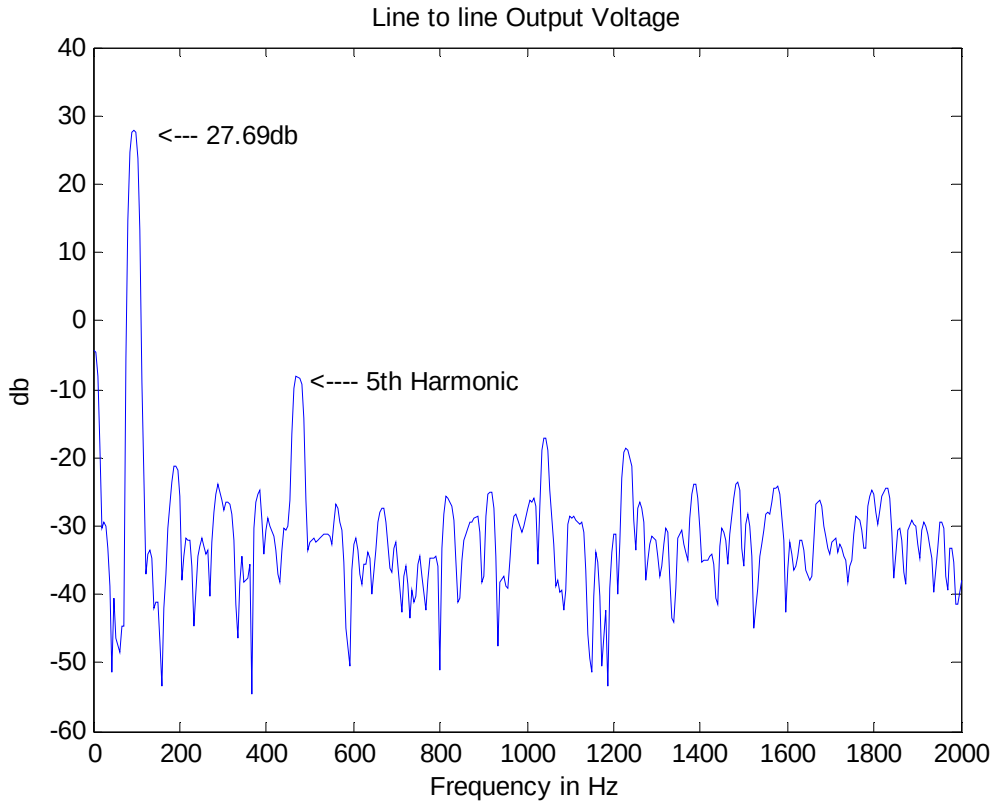


Figure 37. Output Voltage Spectrum.

Notice the large value of the fifth harmonic in Figure 37. The system model results, presented earlier, correctly predict a large value for the fifth harmonic.

2. Blanking Time Compensation

The blanking time compensation code was inserted and the gate signal spectrum analysis is presented in Figure 38. The THD of the new gate signal **-49.11dB** is nearly identical to the previous gate signal without blanking time compensation. This shows the compensation code does not have a negative effect on the PWM switching scheme. The success of the blanking time compensation code on the overall system performance can now be analyzed.

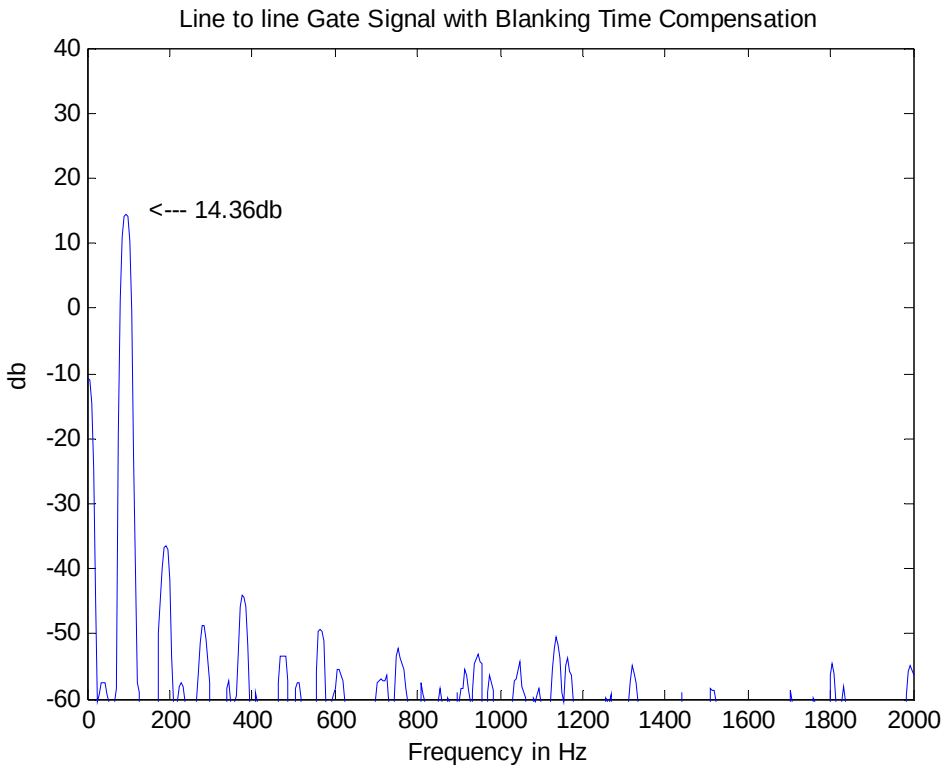


Figure 38. Gate Signal output with Compensation Code.

The insertion of the blanking time compensation code produces the line to line output voltage in Figure 39. The noise floor is raised considerably and the fifth and seventh harmonics are not significantly decreased.

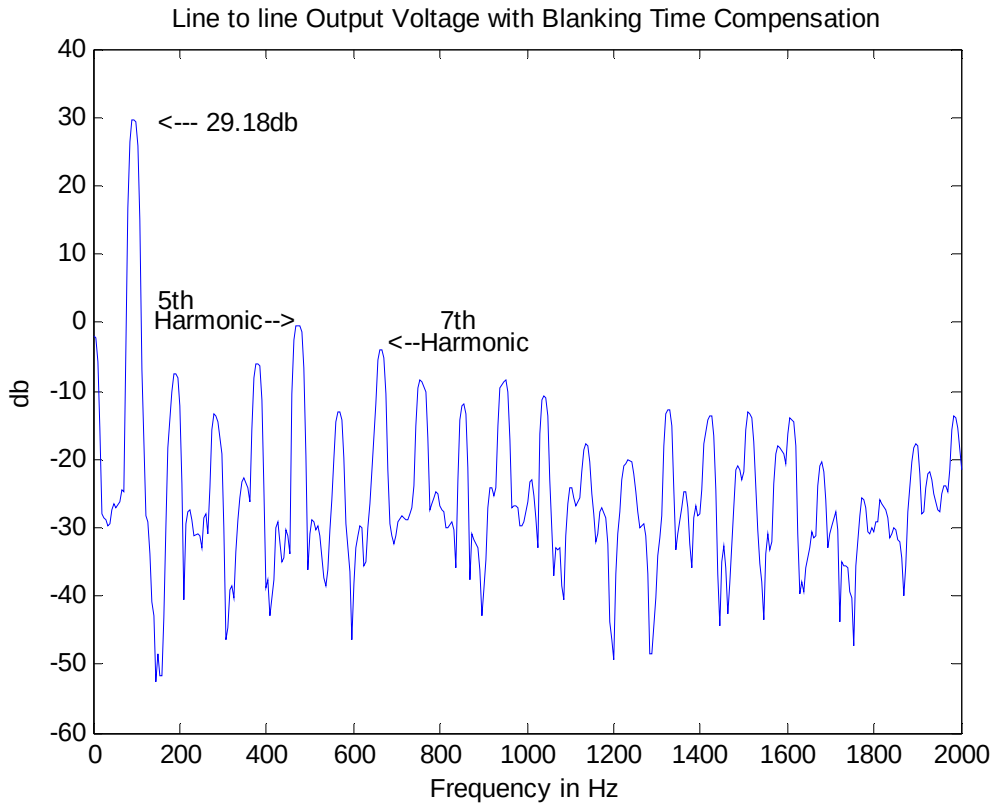


Figure 39. Spectrum with blanking time correction.

The blanking time compensation code did not improve the system performance as anticipated. The measured THD for the system was **-26.3dB**. Even though the compensation code effectively corrected the delay associated with blanking time the THD for the system has not been improved. The compensation did however increase the amplitude of the fundamental in the voltage output. The value rose from **27.69dB** without compensation to **29.19dB** with compensation.

One possible cause for the lack of improvement in the THD is the ripple across the DC bus. The output voltage ripple refers to the difference in the instantaneous values of the waveform and its fundamental-frequency component [8]. One method to reduce the impact of this problem is to add more capacitors across the DC bus. This approach is explored in the next section.

3. Feedback Capacitors Inserted

Two 3500μF capacitors were inserted in parallel across the DC Bus in an attempt to reduce the ripple across the Bus. The output spectrum across the DC bus without the capacitors inserted is shown in Figure 40. These harmonics have relatively little effect on the output voltage spectrum.

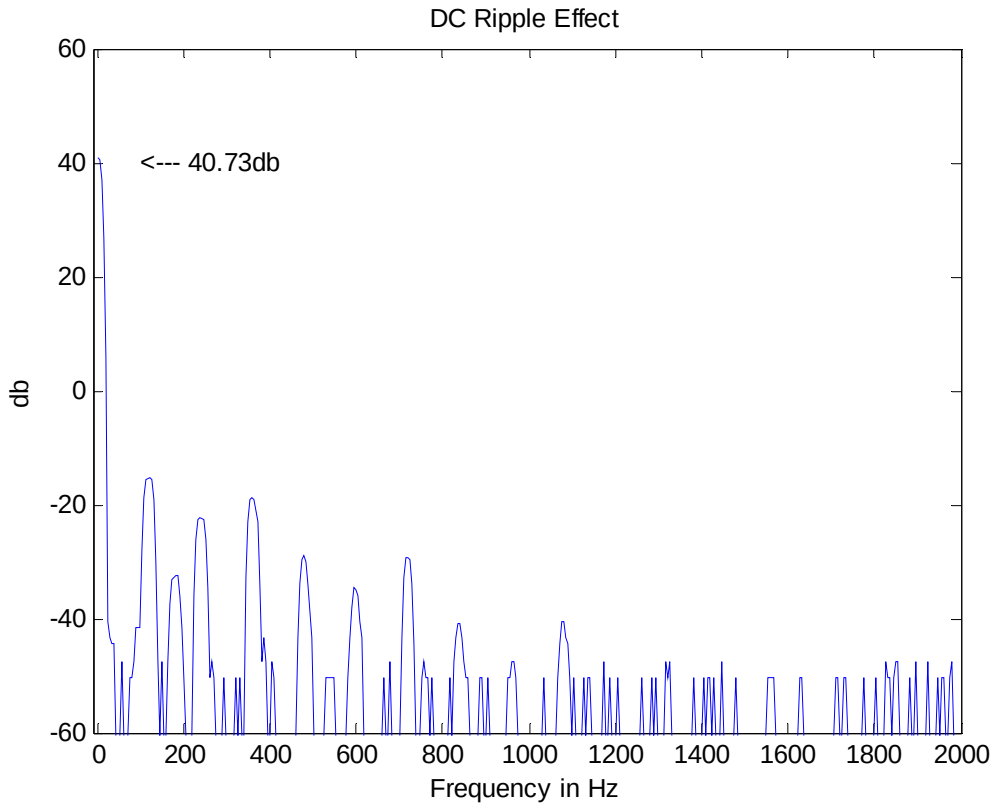


Figure 40. Output Spectrum Across the DC Bus without Capacitors

The output voltage across the DC Bus with the feedback capacitors inserted is shown in Figure 41. In comparison to the previous figure (Figure 40) this represents an improvement.

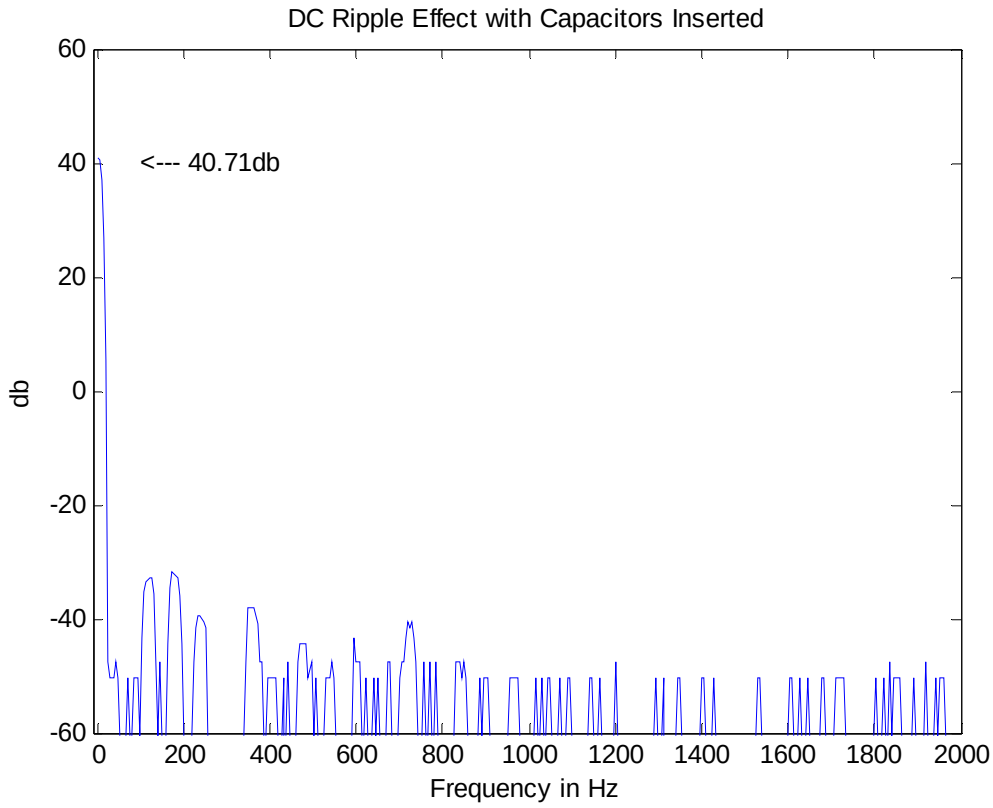


Figure 41. Output Spectrum Across the DC Bus with Capacitors

The capacitor's impact on the line to line output spectrum is unnoticeable. The result from this experiment (Figure 42) is very similar to the previous results shown in Figure 39. The addition of DC bus capacitors slightly reduced the overall system THD to **-27dB** from **-26.3dB** without the capacitors. The voltage ripple on the DC bus does not significantly contribute to the line to line output voltage distortion. Figure 42 displays the line to line output spectrum with the capacitors inserted and the blanking time compensation code.

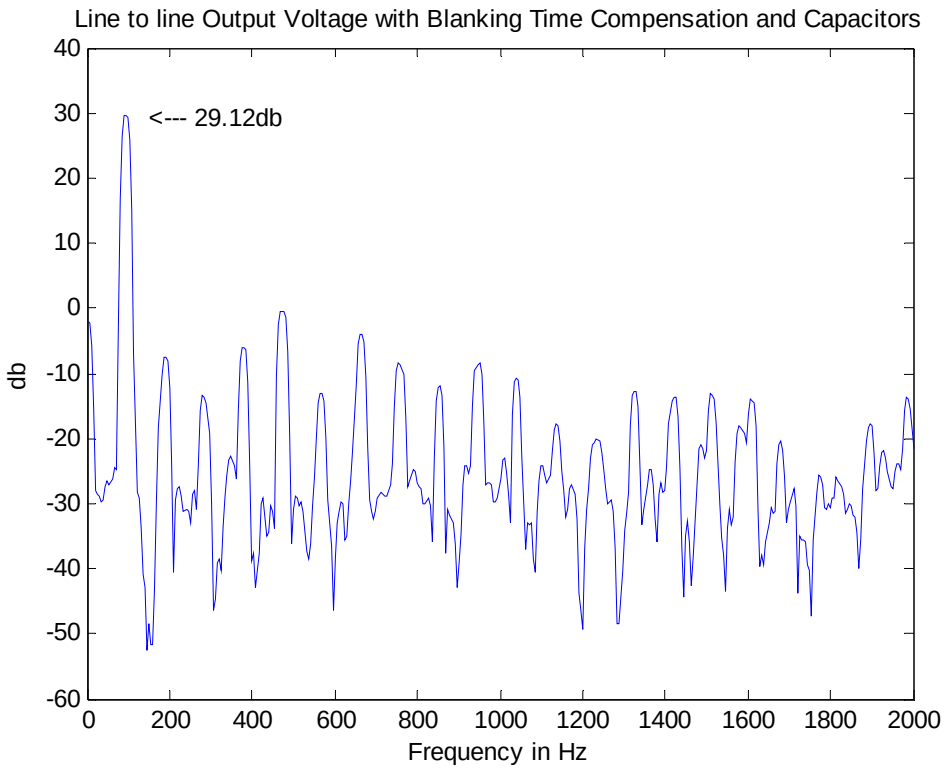


Figure 42. Line to line with Capacitors inserted.

The overall system setup is shown in Figure 43, less the three-phase wye connected load which was previously displayed in Figure 28.

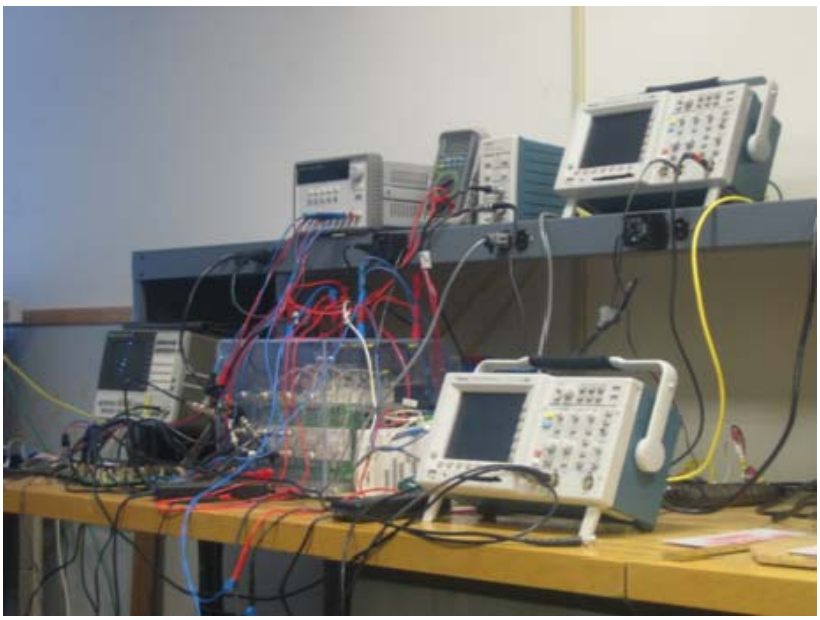


Figure 43. Complete Setup.

D. SUMMARY

This chapter presented the results from testing the compensator code logic in the laboratory. The compensation code corrected the delay associated with blanking time. However, the compensation code did not perform as expected with respect to the THD of the line to line output voltage, even though the simulated results predicted otherwise. The compensation code did not improve THD of the line to line output voltage. The next chapter will discuss conclusions from testing and possible areas for improvement.

VI. CONCLUSIONS AND RECOMMENDATIONS

A. OVERVIEW

This chapter presents conclusions from this research effort and suggest several areas for future study.

B. CONCLUSIONS

This thesis successfully completed the following objectives:

- A method was developed to compensate for blanking time delay using SIMULINK® software embedded in an FPGA.
- A Model of the Semikron SemiTeach IGBT system was created and was utilized to predict the effectiveness of the blanking time compensation code.
- The blanking time compensator code was tested by simulation and laboratory experiments
- The NPS custom printed circuit board was used to interface with the Virtex II^{TM} FPGA in order to test the compensation method.

The THD for the system was not reduced even though the delay associated with blanking time was compensated for, from this it can be inferred blanking time distortion is not the most dominant source of distortion in the Semikron VSI module. Other possible causes could be the forward voltage drop across the switching devices. The capacitance across each inverter leg may also contribute to the inverter distortion.

C. FURTHER STUDY

There are several areas that could further research areas presented in this thesis they include but are not limited to the following:

- Implementing an effective method to compensate for the distortion caused by the forward voltage drop of the switching devices.
- Explore the distortion caused by the capacitance in the switching devices
- Closing the control loop; the system model and PWM scheme was done with an open loop system. Closing the control loop is a possible method to improve system performance

- The system model and laboratory experiments were conducted at relatively low voltage. Future work could model the system and perform experiments at higher voltages.

The opportunities for further study listed above provide areas for others to explore and create methods for further compensating for distortion in PWM voltage source inverters and thereby generate cleaner power.

APPENDIX A. MATLAB® CODE AND SIMULINK® SCHEMATICS

A. SIMULINK® MODEL INITIALIZATION M.FILES

Initialization M.File

```
Vdc=90;
Kp_i=.01/6*Vdc/sqrt(3)/2;%current PI gain is amplified to account for
the SV modulation scaling
Ki_i=3*Vdc/sqrt(3)/4;    %Current control loop gain
Kp_v=.5/30*40;
Ki_v=.3*200;
Vdc_comp=30;
Vcesat=2.3;
Vdc=350;
%delaycount=480;
delaycount=1;
oversample=1;  %1 4 work
fin=100;
pulsect = 2400/oversample;
%step_ct=8;
step_ct=1;
delay_ct=84/step_ct;        %blanking time
tstep = 40e-9*step_ct;
clkPeriod=tstep;
mod_index=.75;
F_mat = [0 0 0 1;1 1 2 0;2 2 3 0;3 3 0 0];
O_mat = F_mat;
s1=2*pi*1;
s2=2*pi*5000;
s3=2*pi*50000;
alpha=.0002*sqrt(3)/Vdc/2;
Lfa=2200e-6;
Lfb=Lfa;
Lfc=Lfa;
Cf= 30e-6/10;
Cfa=Cf;Cfb=Cfa;Cfc=Cfb;
Loa=100e-4;
Lob=Loa;Loc=Loa;
Roa=20/1;
Rob=Roa;
Roc=Roa;
Amat_indI = -inv([Lfa -Lfb;Lfc Lfb+Lfc])*.05*[1 -1;1 2];
Bmat_indI = inv([Lfa -Lfb;Lfc Lfb+Lfc]);
Cmat_indI = [1 0 ;0 1 ;-1 -1 ];    %Ic = -Ia-Ib
Dmat_indI = zeros(3,2);
Amat_caps = zeros(3);
Bmat_caps = [1/Cfa 0 0; 0 1/Cfb 0; 0 0 1/Cfc];
Cmat_caps = eye(3);
Dmat_caps = zeros(3);
```

Filter Values

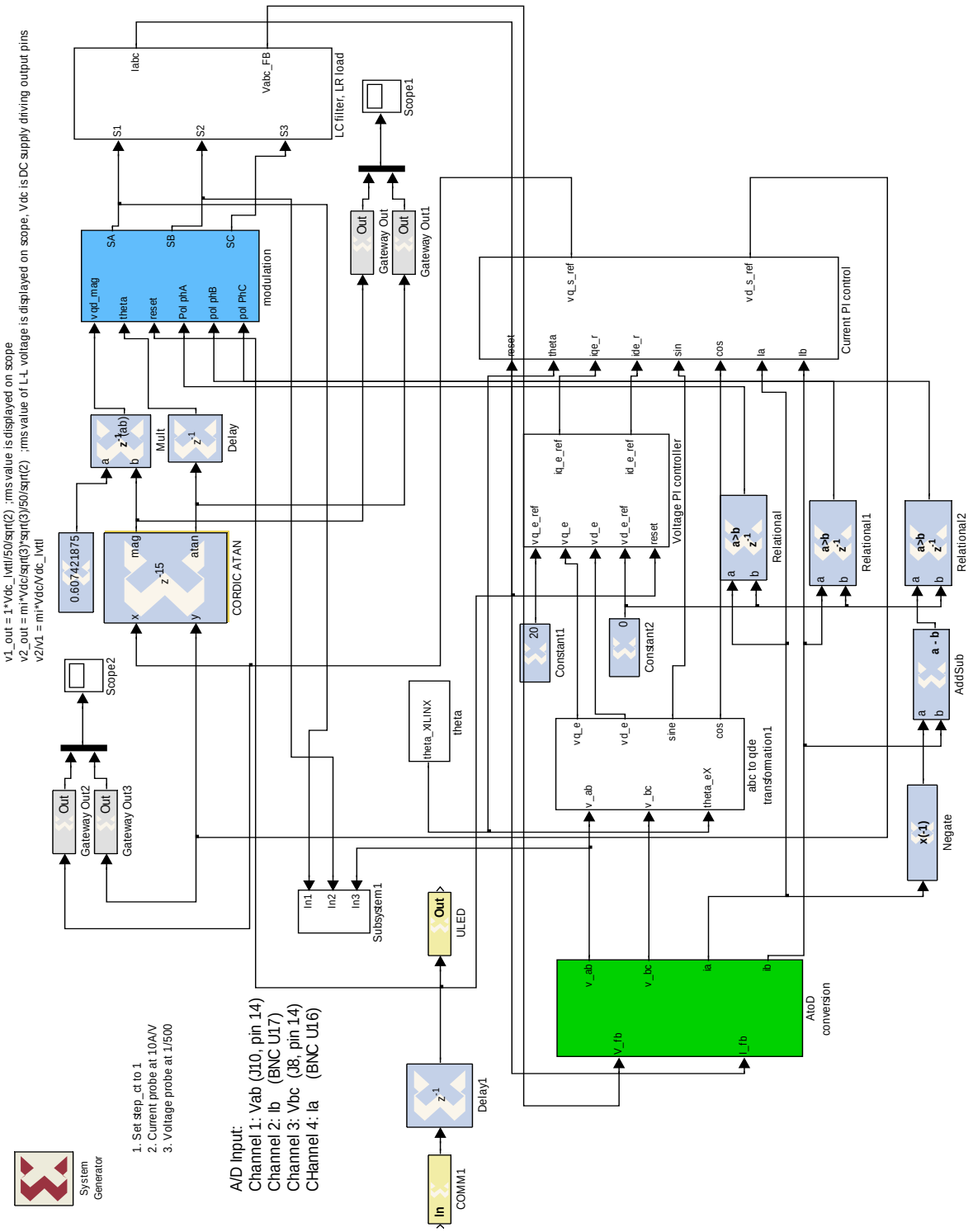
```
Tsample=1/(24e6/170);
beta=(2*pi*1000)^2;
alpha=2*.8*sqrt(beta);
A_coeff=(2/Tsample)^2+alpha*2/Tsample+beta;
B_coeff=-2*(2/Tsample)^2+2*beta;
C_coeff=(2/Tsample)^2-alpha*2/Tsample+beta;
M_coeff=beta/A_coeff;
N_coeff=2*beta/A_coeff;
O_coeff=M_coeff;
P_coeff=B_coeff/A_coeff;
Q_coeff=C_coeff/A_coeff;
[output1, output2]=maxflat(3,3,.01);
A_N=output1(1);
B_N=output1(2);
C_N=output1(3);
D_N=output1(4);
A_D=output2(1);
B_D=output2(2);
C_D=output2(3);
D_D=output2(4);
fvtool(output1,output2)
```

Simulation M.File

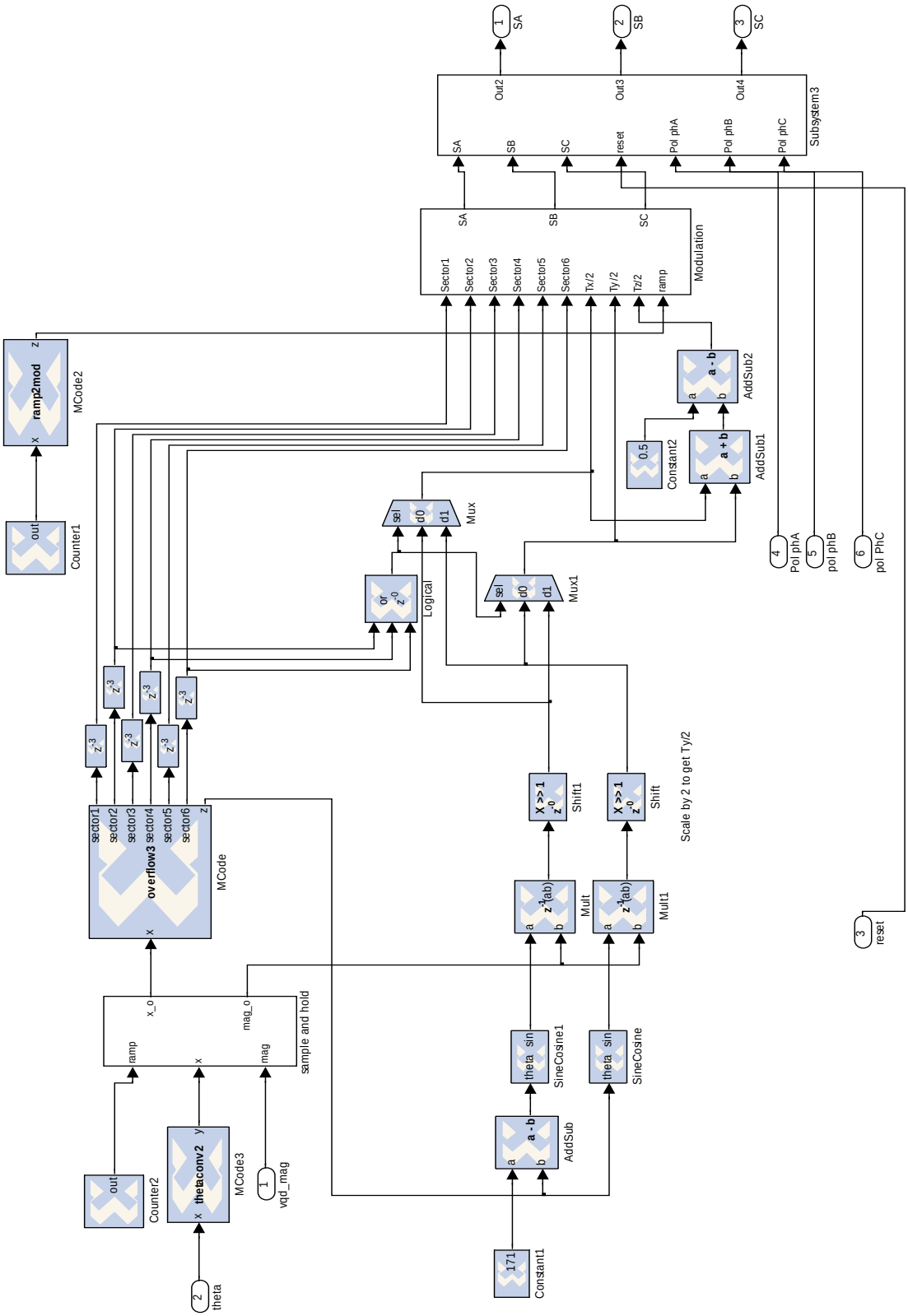
```
clear all;
Vcesat=2.5;
Vd=2.0;
%Vcesat=0;
%Vd=0.001;
Vdc=90;
%Vdc=90;
td_on=70e-9;
td_off=400e-9;
Tsw = 100e-6;
f_fund = 95;
oversample=2;    %Set oversample to an integer to update PWM timer
values more frequently
tstep = Tsw/400;
cycles=5;        %needs to be divisible by 4
tstop=cycles/f_fund;
tblank=4e-6;
%tblank=tstep;
%deltaV=(tblank+td_on-td_off)/100e-6*(Vdc-Vcesat+Vd)+(Vcesat+Vd)/2;
f_filter=50000;  %low pass filter for current feedback

%Vref= 190;
Vref= 26;
%Vref= 30;
Lfa=1200e-6;
Lfb=Lfa;
Lfc=Lfa;
Roa=20;
Rob=Roa;
Roc=Roa;

Amat_indI = -inv([Lfa -Lfb;Lfc Lfb+Lfc])*Roa*[1 -1;1 2];
Bmat_indI = inv([Lfa -Lfb;Lfc Lfb+Lfc]);
Cmat_indI = [1 0 ;0 1 ;-1 -1 ];    %Ic = -Ia-Ib
Dmat_indI = zeros(3,2);

one_zero_state=0;       %Set to one so that only one zero state is used
in modulation
if one_zero_state == 1
    gain1 = 1;
    gain2 = 0;
else
    gain1 = 1/2;
    gain2 = 1;
end

col1=[0;Vd;Vd;Vd;-Vcesat;-Vcesat;-Vcesat;0];
col2=[0;Vcesat;-Vd;-Vd;Vcesat;Vcesat;-Vd;0];
col3=[0;-Vd;Vcesat;-Vd;Vcesat;-Vd;Vcesat;0];
col4=[0;Vcesat;Vcesat;Vcesat;-Vd;-Vd;-Vd;0];
col5=[0;Vd;-Vcesat;-Vcesat;Vd;Vd;-Vcesat;0];
col6=[0;-Vcesat;Vd;-Vcesat;Vd;-Vcesat;Vd;0];
Dist_mat1=[col1 col2 col3];
Dist_mat2=[col1 col5 col3];
Dist_mat3=[col4 col5 col3];
```

```
Dist_mat4=[col4 col5 col6];
Dist_mat5=[col4 col2 col6];
Dist_mat6=[col1 col2 col6];
Ks=2/3*[1 -1/2 -1/2;0 -sqrt(3)/2 sqrt(3)/2;1/2 1/2 1/2];
```

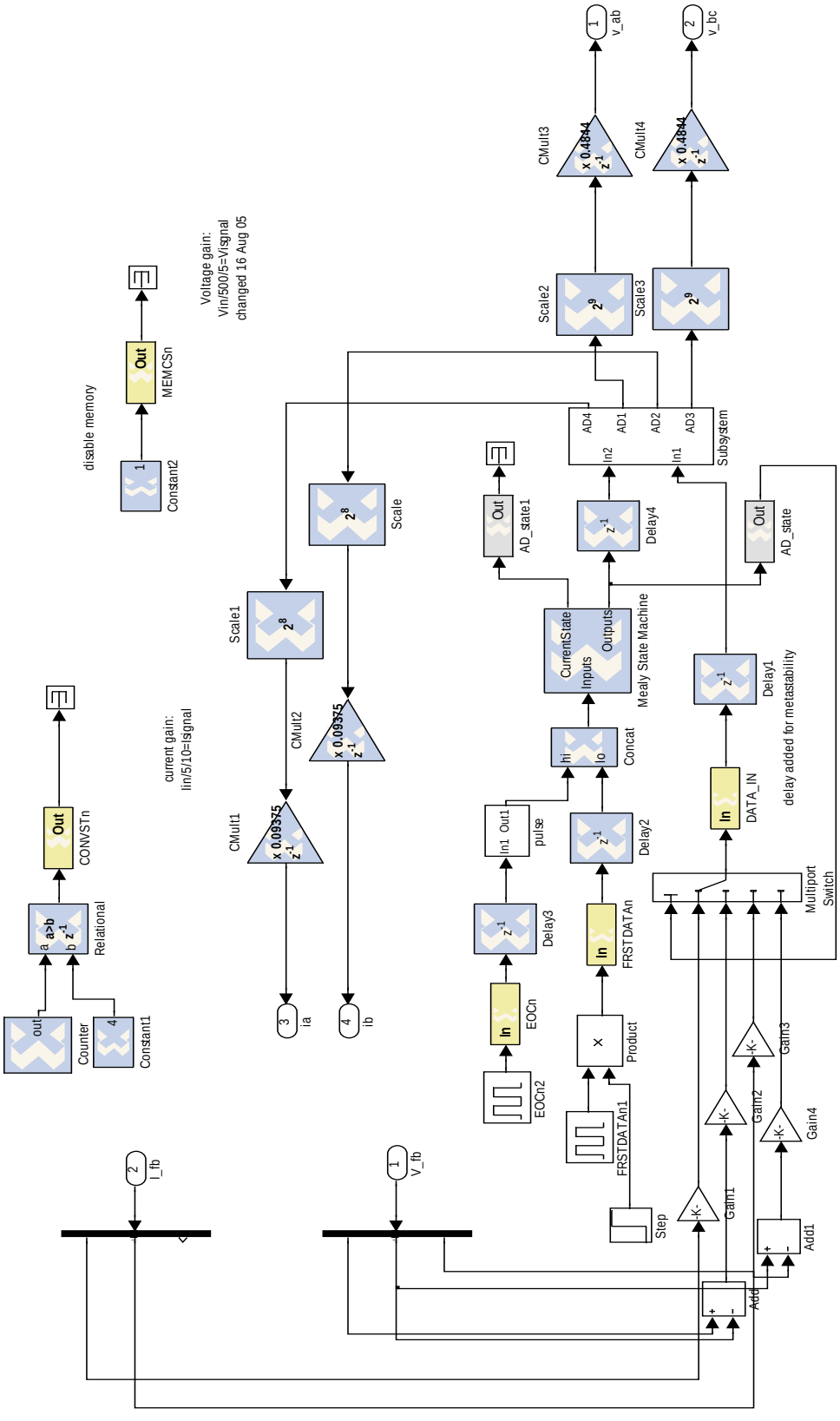
B. SIMULINK® BLOCK SCHEMATICS



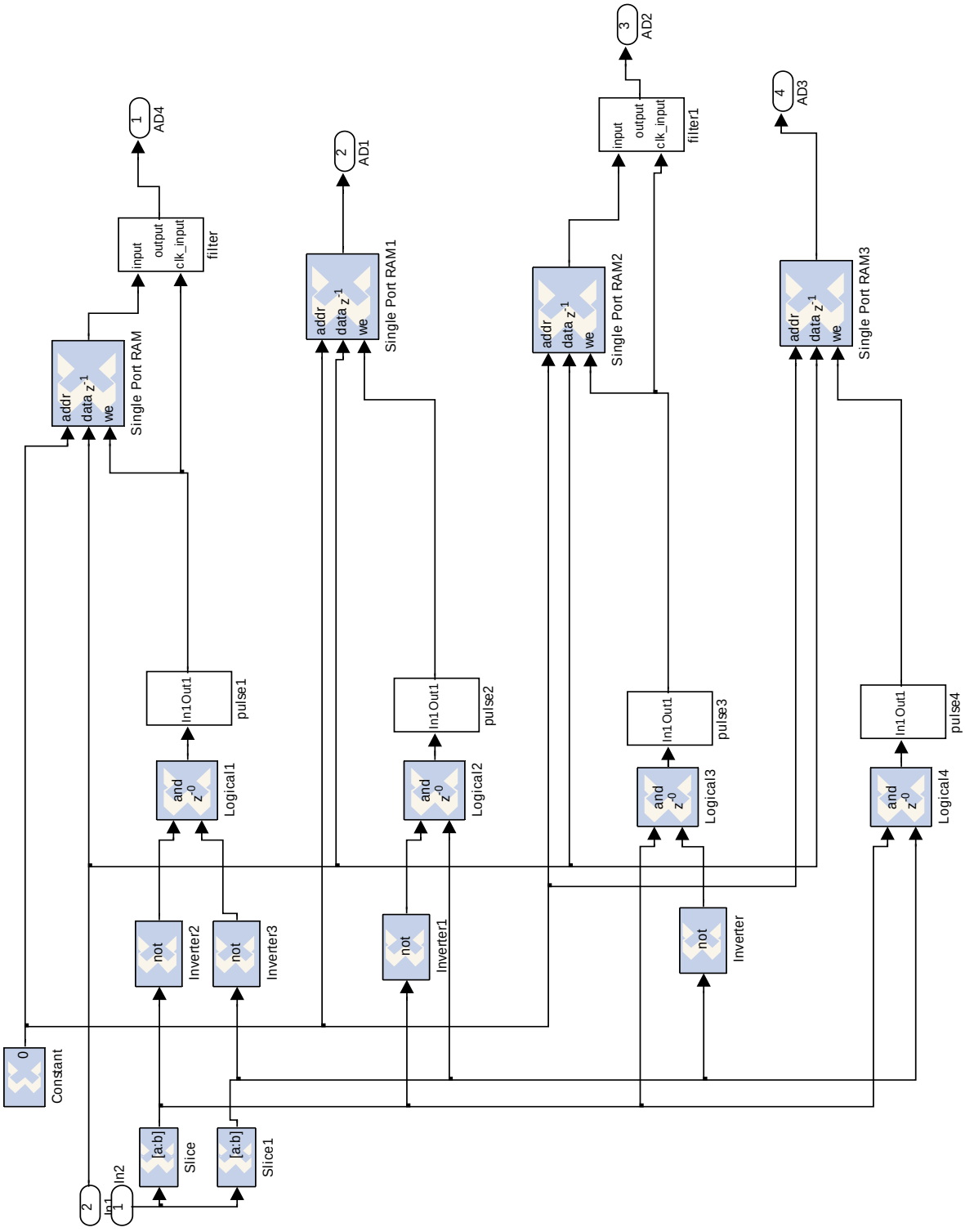
Top level Model design



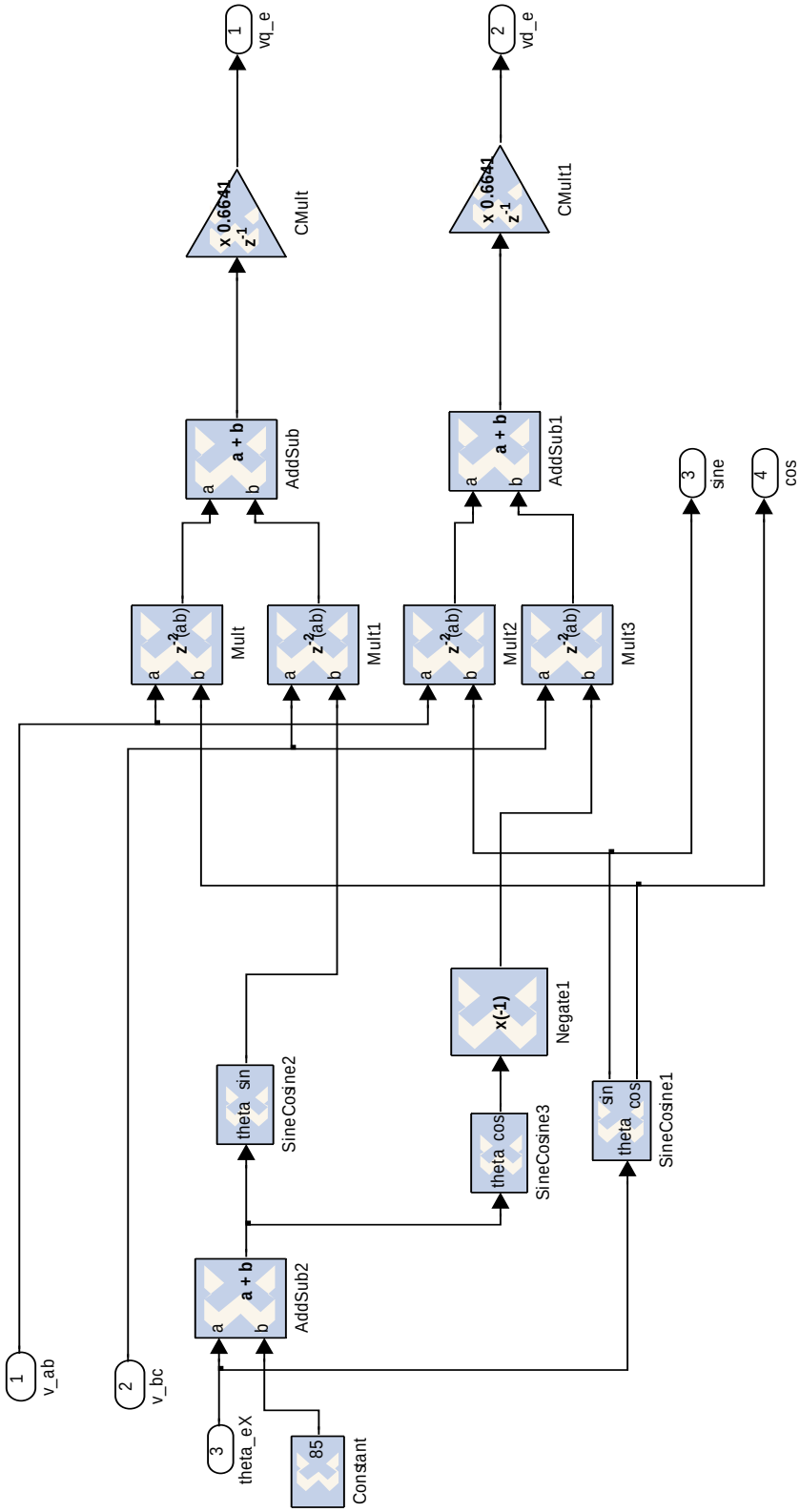
Modulation Subsystem



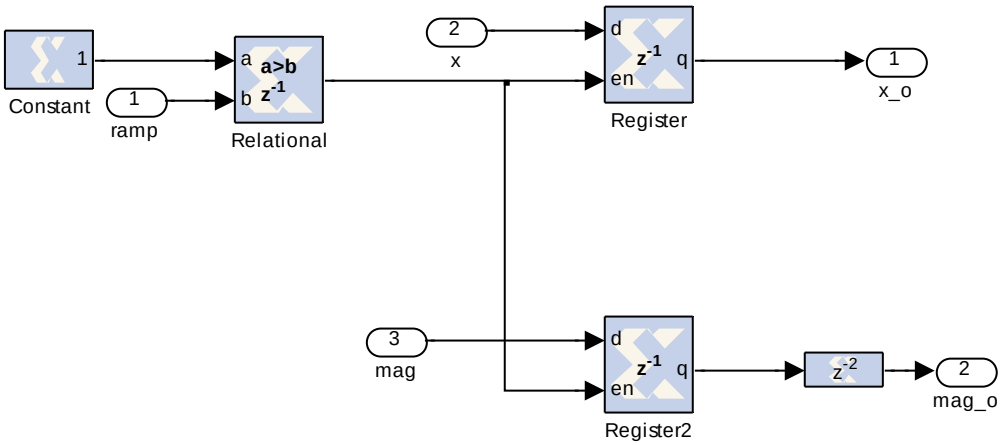
Analog to Digital Converter Subsystem



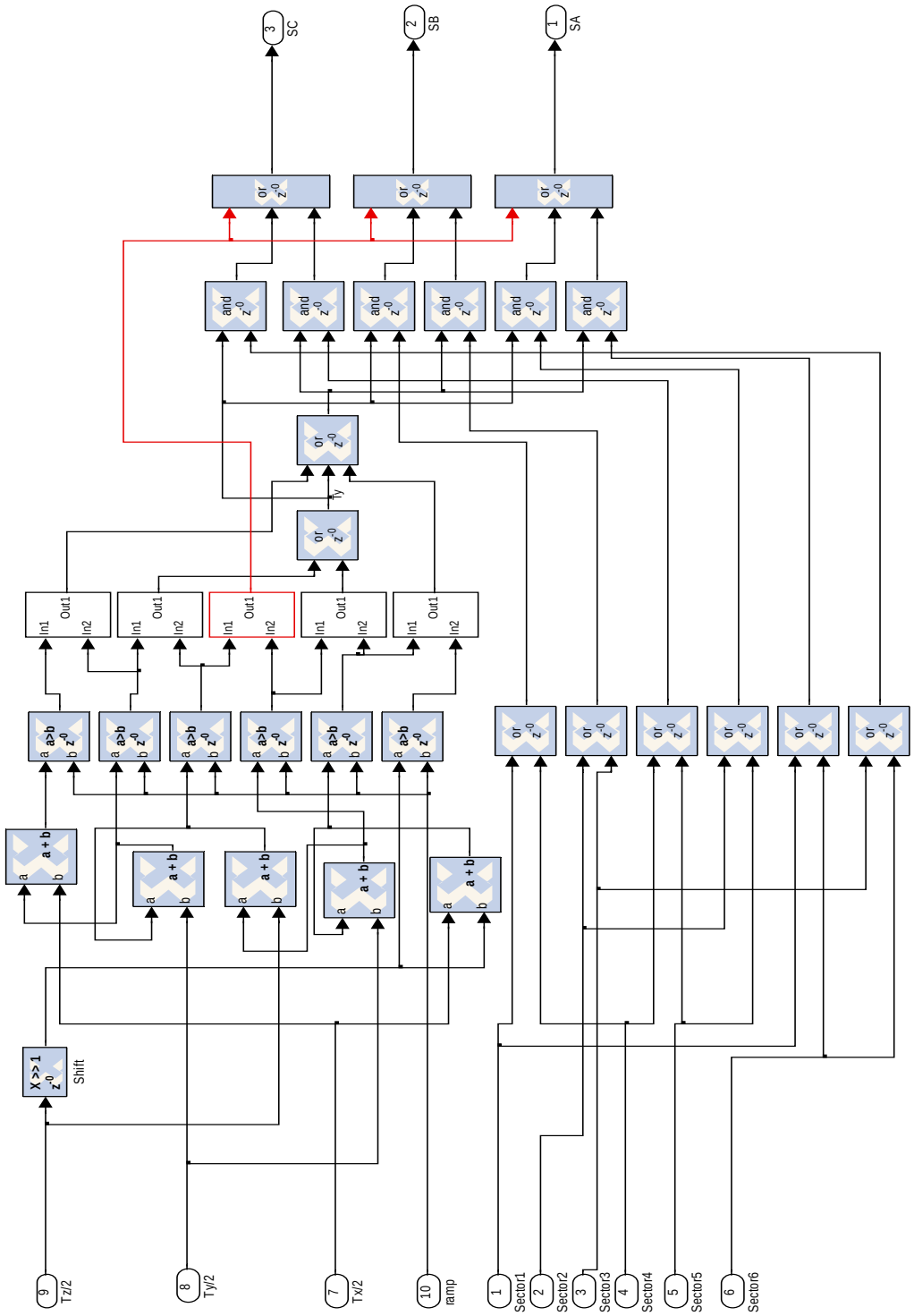
Analog to digital converter Subsystem 2



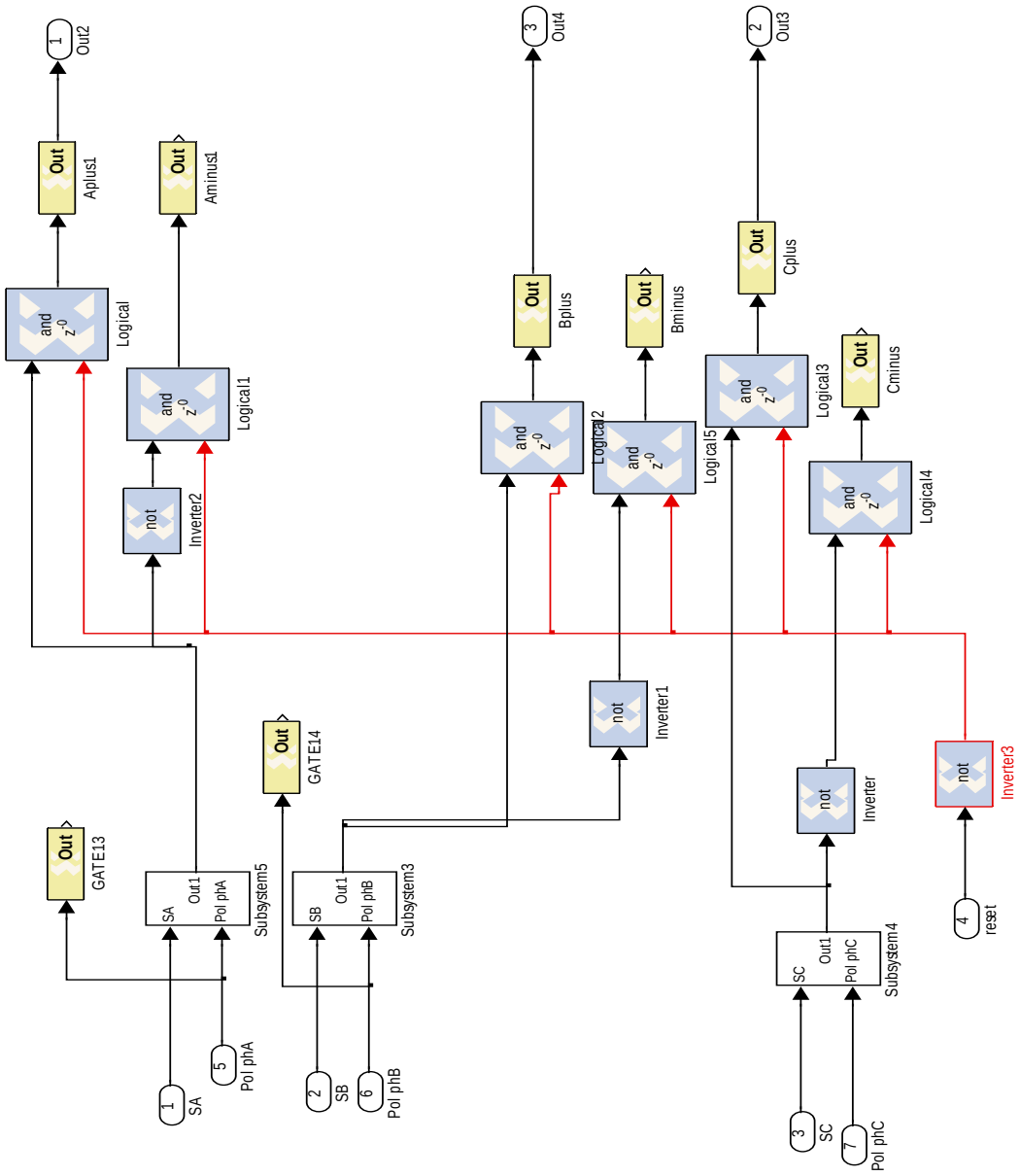
ABC to QDE Transformation Block



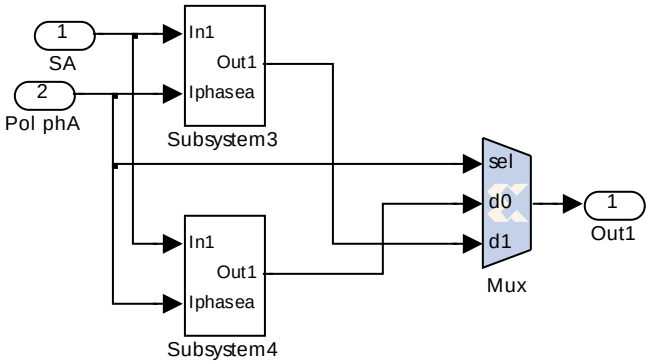
Sample and Hold Block



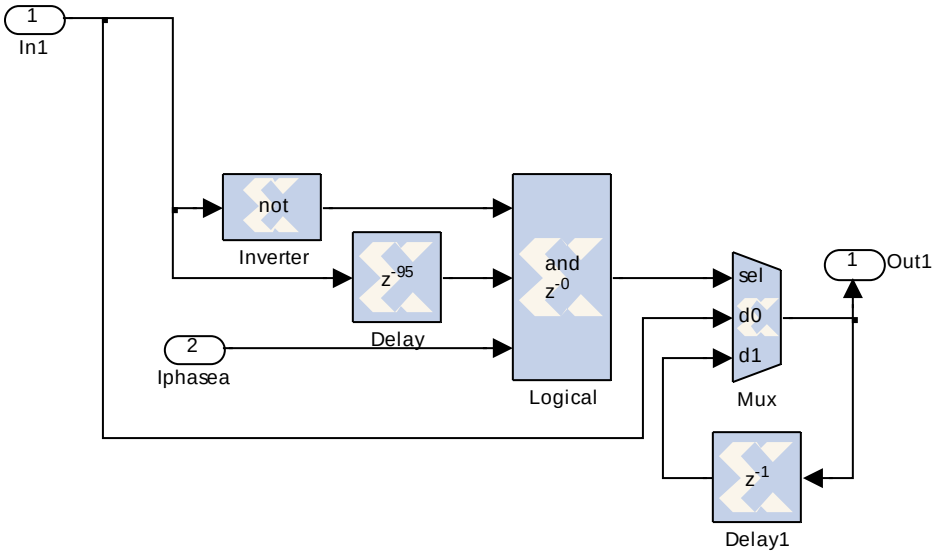
Gate Signal Generator Block



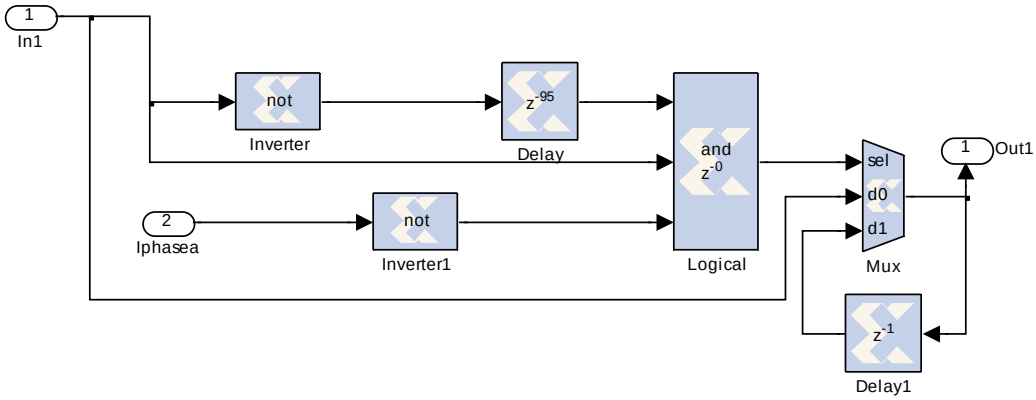
Gate Signal Output Block



Blanking time code insertion Block

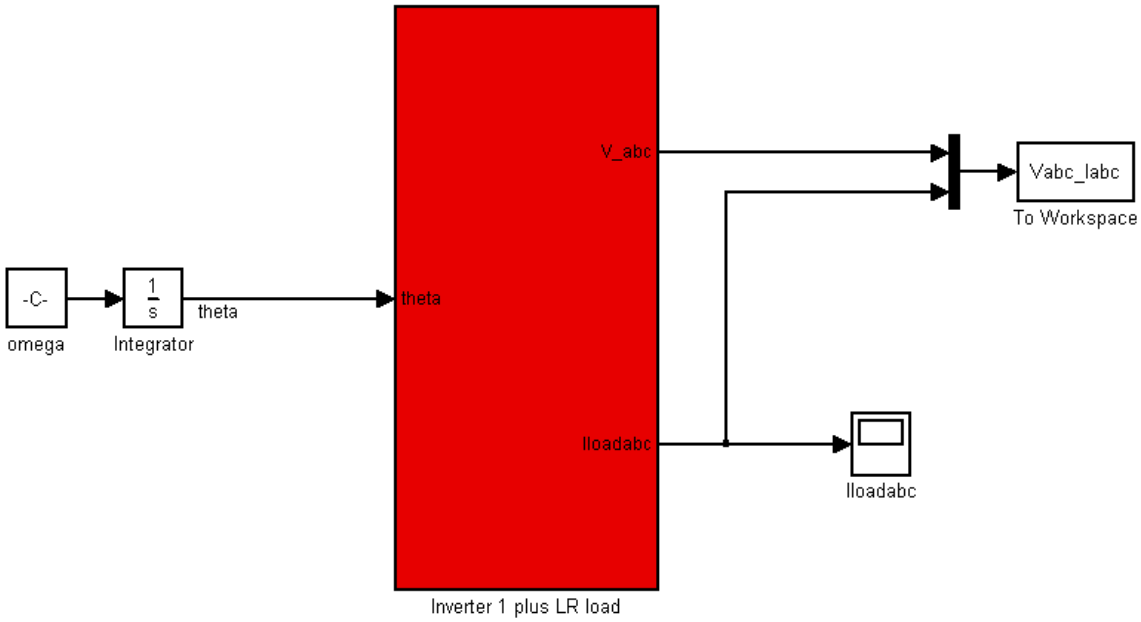


Positive Current Blanking time Correction

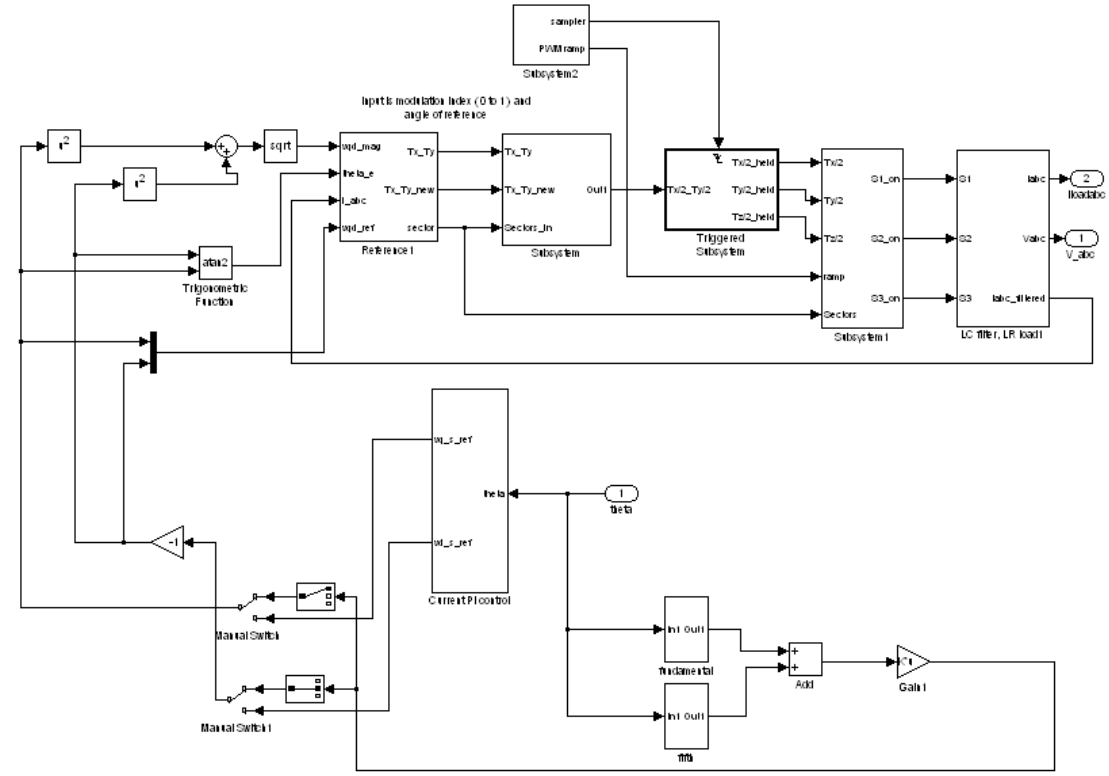


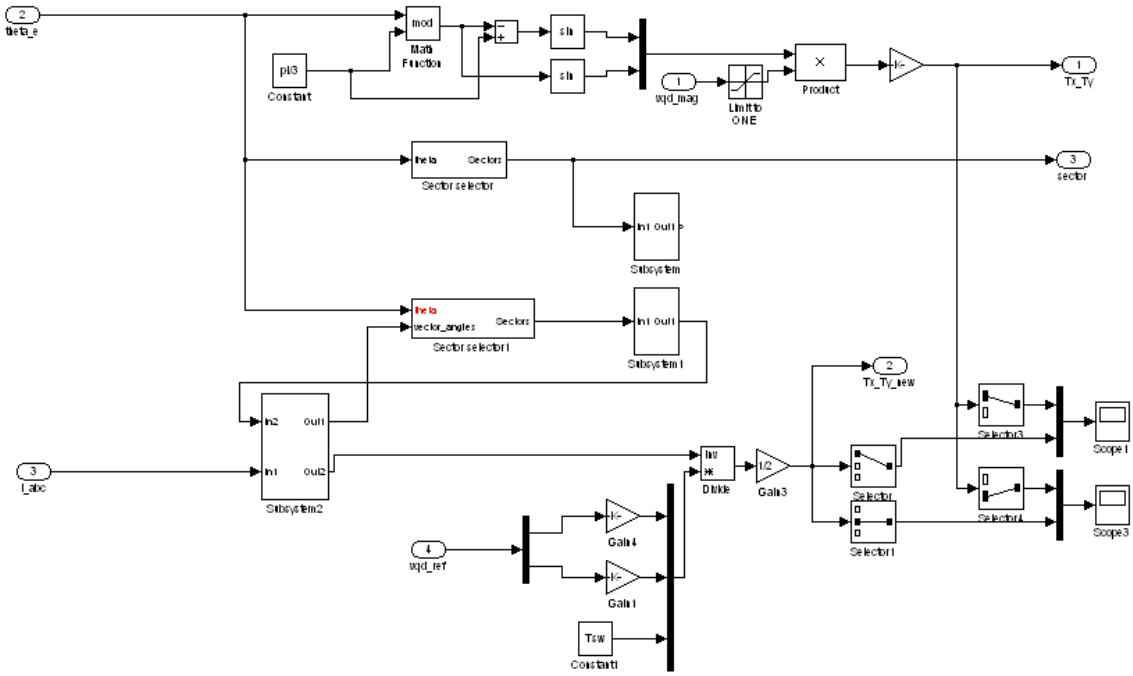
Negative Current Blanking Time Correction Block

Simulation Model Overview

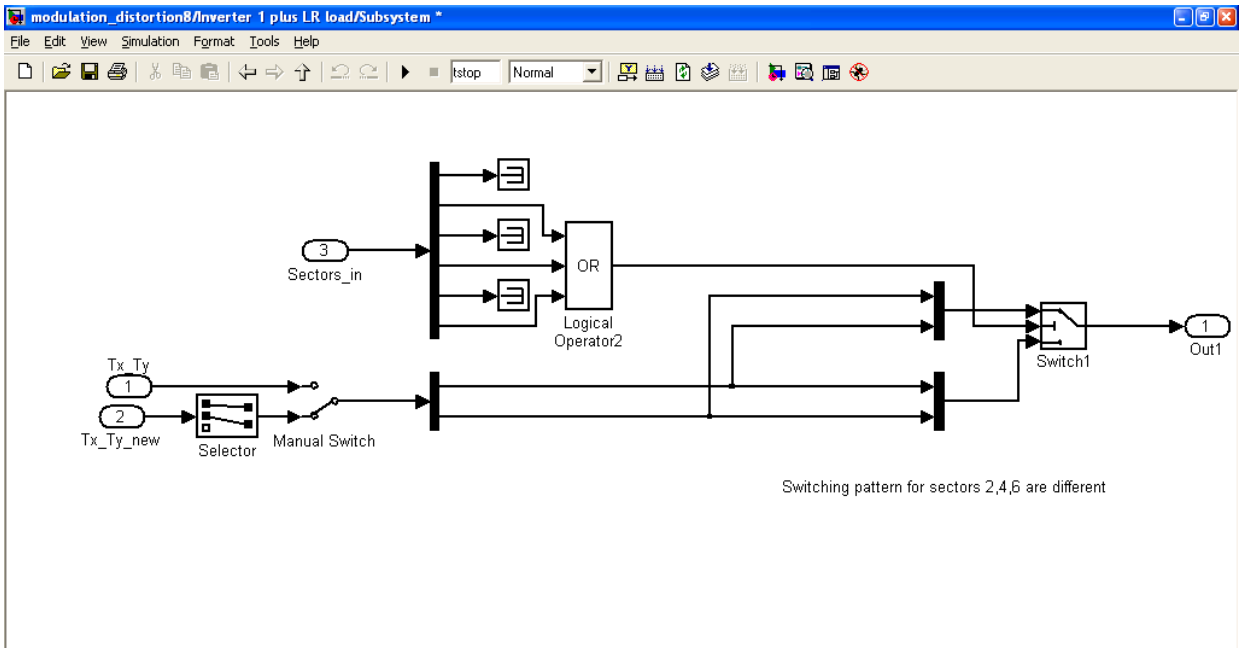


Inverter 1 Plus RL Load

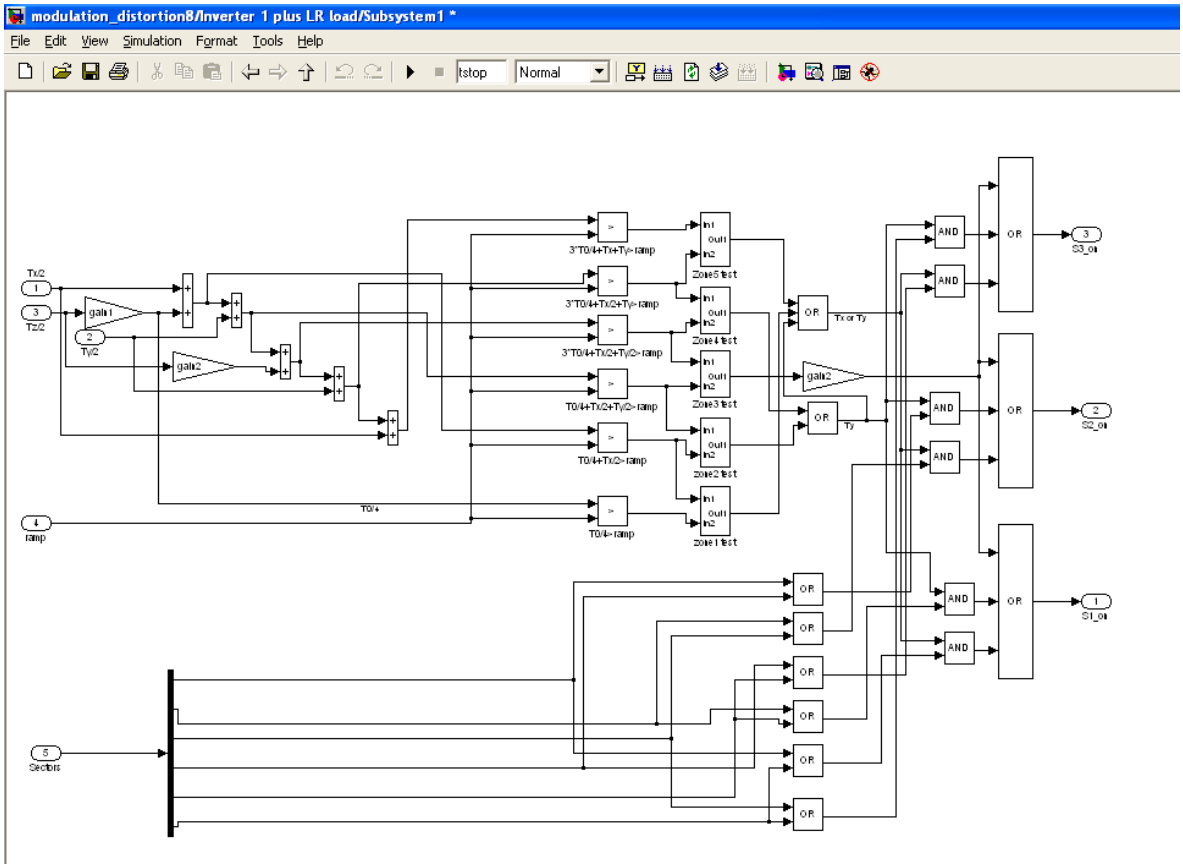




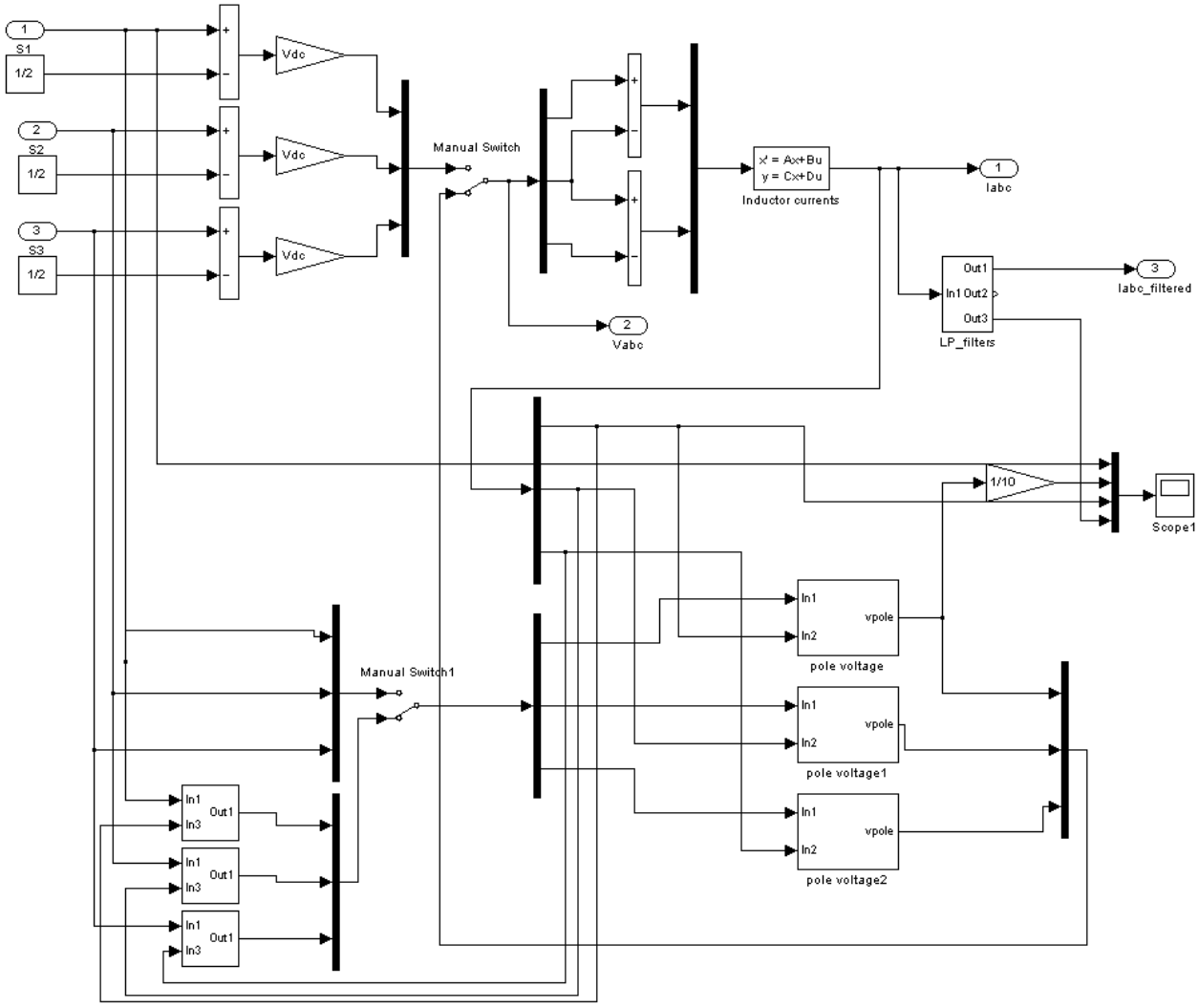
Inverter 1 Plus RL Load Manual Switch Subsystem



Gate Signal Generator



RL Load and Distortion Blocks



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APPENDIX B. CIRCUIT BOARD LAYOUTS AND PARTLISTS

A. FPGA DATA SHEET

Memec Design

Virtex™-II LC1000 Development Kit

Product Brief

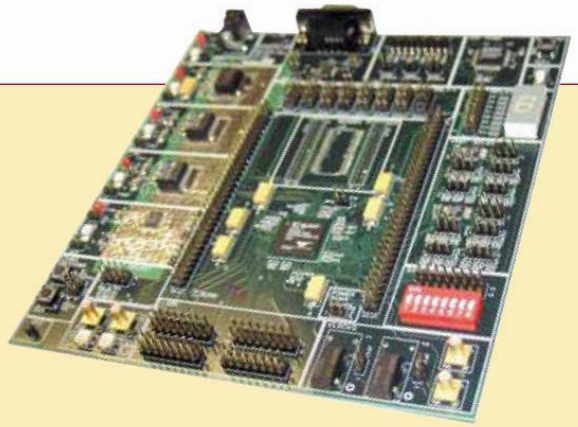
The Virtex-II LC1000 Development Kit verifies platform FPGA design applications.

Features

- Easy to use development platform
- Based on the Xilinx® 1 M gate Virtex-II FPGA (XC2V1000)
- User I/O expansion connectors
- Bank selectable reference voltage and resistors to support multiple I/O standards
- Supports four clock inputs
- Two user clock outputs via SMB connectors
- High performance 32 MB DDR memory
- LVDS transmit and receive ports
- Low cost and high flexibility

Applications

- General-purpose prototyping platform
- Digital signal processing
- Telecommunication and networking
- Video and wireless



Product Description

The Virtex-II LC1000 Development Kit provides an easy to use development platform for prototyping and verifying Virtex-II based designs. The Virtex-II family is a platform FPGA intended for high performance, low to high-density designs with IP cores and customized modules. The Virtex-II family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications. In addition to performance and density, the Virtex-II family offers many supported I/O standards, external interfaces for PCI-X, QDR and DDR, abundant memory resources and on-chip multipliers, features that enable FPGA designers to meet the design requirements of next generation telecommunication and networking applications. The Virtex-II reference board employs the Xilinx 1 M gate Virtex-II (XC2V1000) device. The reference board's supporting devices work in conjunction with the Xilinx Virtex-II FPGA to facilitate the prototype of high-performance memory and I/O interfaces such as differential signaling (LVDS) and high-speed DDR memory interfaces.

Virtex-II also includes a high performance and flexible digital clock manager (DCM) with on-chip digital controlled impedance (DCI) for source/load terminations, a feature that enables FPGA designers to perform high-level integration, reduce board level cost, and improve overall system level reliability and performance. The Virtex-II reference board provides the required test circuits for exploring and testing these functions. Advanced features such as in-system programmability of the on-board ISP PROM, complete high-performance differential signaling support, and the Reference Design Center's pre-configured reference designs make the kit a perfect solution for FPGA and system designers who need a quick, flexible and low cost prototyping platform.

The Virtex-II reference board utilizes the Xilinx XC18V04 ISP PROM, allowing FPGA designers to quickly download revisions and verify design changes so that they can meet the final system-level design requirements. In addition to the ISP PROM, the reference board provides a JTAG connector for direct configuration of the Virtex-II FPGA.

The Virtex-II reference board is bundled with VHDL and Verilog HDL reference design examples to help FPGA designers shorten development time and meet time-to-market requirements.

Virtex™-II LC1000 Development Kit

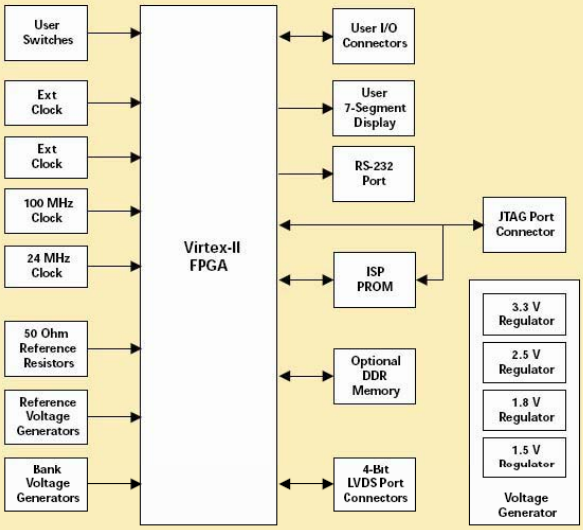
MDS008-03 02/10/03 ©Memec, LLC

Contact Memec: xilinx.info@memecdesign.com 888.488.4133 x212 (North America Only) or 858.314.8190 (Outside US)

Memec Design

Virtex-II LC1000 Development Kit Includes:

- Virtex-II Reference Board
  - 1 M gate Virtex-II FPGA device (XC2V1000-4FG256C)
  - 3.3 V, 2.5 V, 1.8 V and 1.5 V on-board voltage regulators
  - XC18V04 ISP PROM
  - On-board 32 MB DDR memory
  - RS-232 port
  - User switches and user I/O ports
  - Seven-segment LED display
  - LVDS transmit and receive ports
  - Eight-bank SelectI/O voltage (VCCO) settings (1.5 V, 1.8 V, 2.5 V and 3.3 V options)
  - Eight-bank reference voltage (VREF) settings (1.5 V, 1.25 V, 1.0 V, 0.90 V and 0.75 V options)
  - Bank reference resistors to support DCI
  - Two on-board clock sources and two SMB user clock inputs
  - Two user SMB clock output connectors
  - JTAG port
- AC-to-DC power supply adapter
- Complete reference designs with source code (VHDL and Verilog HDL)
- Bundled software options



Ordering Information

	Americas Part #	International Part #
Virtex-II LC1000 Development Kit		
Virtex-II Development Kit	DS-KIT-V2LC1000	DS-KIT-V2LC1000-EURO
Kit with ISE Alliance and JTAG Cable	DS-KIT-V2LC1000-ALI	
Kit with ISE Foundation and JTAG Cable	DS-KIT-V2LC1000-ISE	

Virtex™-II LC1000 Development Kit

B. POWER ELECTRONICS TEACHING SYSTEM DATA SHEET

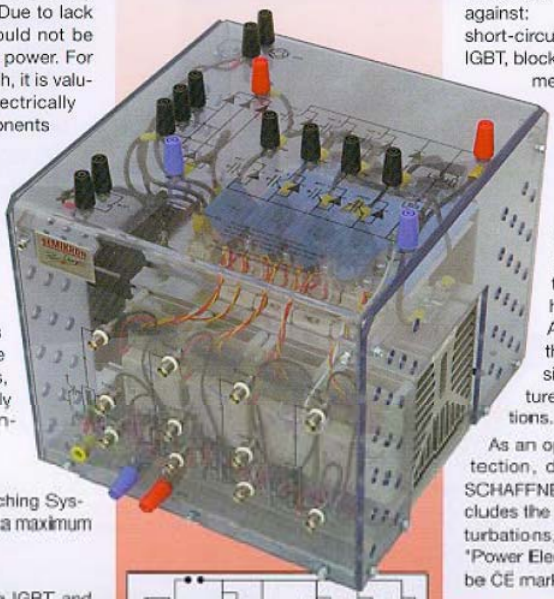
!NEW!

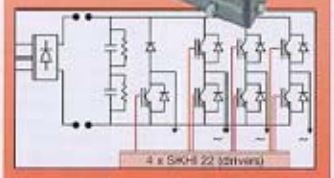
SEMIKRON
innovation+service

Power Electronics Teaching System

IGBT demonstration converter for schools and universities

When teaching and demonstrating the exciting world of power electronics , safety must be the main concern. Due to lack of experience, students should not be exposed immediately to live power. For a better understanding though, it is valuable to actually see and electrically access the individual components of the system.
The new "Power Electronics Teaching System" from SEMIKRON achieves exactly this.
The "Power Electronics Teaching System" will meet various application requirements regarding converters up to 20 kVA : 3 or 1 phase motors, DC current motors, UPS, active filter... or the totally new application you just invented!





Power Design

The "Power Electronics Teaching System" was designed to provide a maximum of 30 A rms per phase.

Major components:

- 3 half-bridges module with IGBT and CAL-diode SKM 50GB123D
  1 IGBT brake chopper SKM 50GAL123D
- a 3-phase diode rectifier SKD 51/14
- DC busbar capacitance of 1100 µF/ 800 V
- 4 SKHI 22 drivers

Output power capability: up to 20 kVA (3 phase)
Switching frequency: up to 20 kHz
Max input AC voltage : 3x480 V~ (400V with filter)

Passive Security

The power converter is protected by a plastic case on which all the standard security connectors for power ("banana" type) and command (BNC type) are fixed. This case offers double IP protection.

Active Security

The driver SKHI 22 protects the IGBTs against:
short-circuits (detection, switch off the IGBT, blocking of all further signals, error message)
under-voltage of the power supply (blocking of all signals, error message), simultaneous command of both IGBTs in one phase-leg (through logic and dead-time).
Furthermore, a thermal protection prohibits destructive heatsink temperatures.
A sensor has been placed at the warmest point of the heatsink to measure the temperature and validate your calculations.

As an option, a complete EMC protection, defined in partnership with SCHAFFNER, can be delivered. This includes the filter against conducted perturbations, this protection allows the "Power Electronics Teaching System" to be CE marked.

Applications Manual/ initial class assignments

With over 40 years of experience SEMIKRON has designed its "Power Electronics Teaching System" to expose students to realistic industrial applications design. The manual also gives an example for an initial educational demonstration. Students can compare the test results with the calculation method in the manual.

SEMIKRON Quality

As a leader in power IGBT power systems, SEMIKRON ensures the quality of your "Power Electronics Teaching System" by providing a final test certificate. Every IGBT of each power stack is tested in short-circuit, at maximum voltage, and the complete stack is tested under full load conditions (max. current, max. DC Voltage).

enables practical demonstrations and makes your projects safer and more efficient
makes the power electronics courses safe and prevents dangerous and expensive failures in your equipment
increases your demonstration time by reducing build-up time

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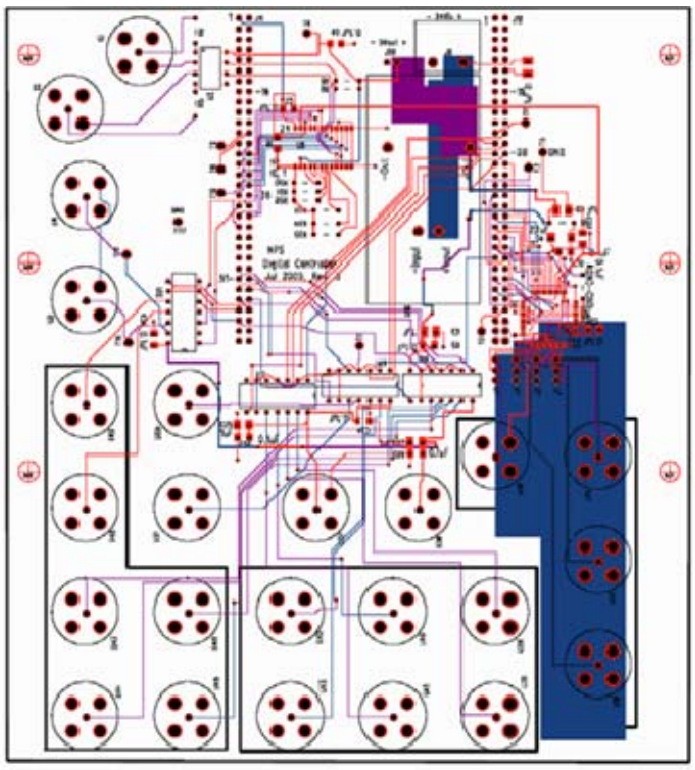
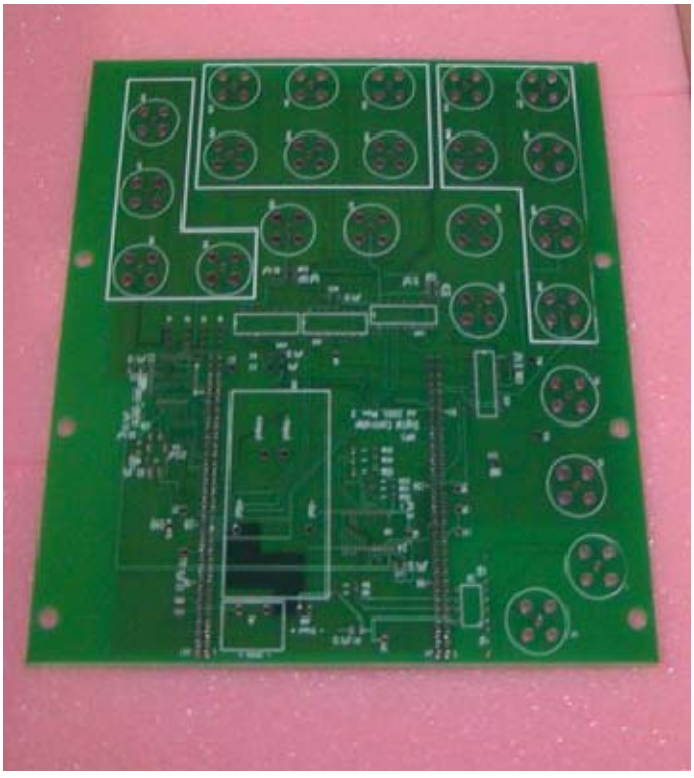
C. INTERFACE BOARD





D. IGBT DRIVER (SKHI21) DATA SHEET

SKHI 22 A / B

SEMIDRIVER™

Hybrid Dual IGBT Driver

SKHI 22 A / B

Preliminary Data

Features

- Double driver for halfbridge IGBT modules
- SKHI 22A is compatible to old SKHI 22
- SKHI 22B has additional functionality
- CMOS compatible inputs
- Short circuit potection by V_{CE} monitoring and switch off
- Drive interlock top / bottom
- Isolation by transformers
- Supply undervotage protection (13 V)
- Error latch / output

Typical Applications

- Driver for IGBT modules in bridge circuits in choppers, inverter drives, UPS and whelding inverters

1) see fig. 6

2) At R_{CE} = 18 kΩ, C_{CE} = 330 pF

Absolute Maximum Ratings

Symbol	Conditions	Values	Units
V_S	Supply voltage prim.	18	V
V_{iH}	Input signal volt. (High) SKHI 22A	V_S + 0,3	V
	SKHI 22B	5 + 0,3	V
$Iout_{PEAK}$	Output peak current	8	A
$Iout_{AVmax}$	Output average current	40	mA
f_{max}	max. switching frequency	50	kHz
V_{CE}	Collector emitter voltage sense across the IGBT	1200	V
dv/dt	Rate of rise and fall of voltage secondary to primary side	50	kV/µs
V_{isolIO}	Isolation test voltage input - output (2 sec. AC)	2500	Vac
V_{isol12}	Isolation test voltage output 1 - output 2 (2 sec. AC)	1500	V
R_{Gonmin}	Minimum rating for R_{Gon}	3	Ω
$R_{Goffmin}$	Minimum rating for R_{Goff}	3	Ω
$Q_{out/pulse}$	Max. rating for output charge per pulse	4[1)]	µC
T_{op}	Operating temperature	- 40 ... + 85	°C
T_{stg}	Storage temperature	- 40 ... + 85	°C

Characteristics T_a = 25 °C, unless otherwise specified

Symbol	Conditions	min.	typ.	max.	Units
V_S	Supply voltage primary side	14,4	15	15,6	V
I_{SO}	Supply current primary side (no load)		80		mA
	Supply current primary side (max.)			290	mA
V_i	Input signal voltage SKHI 22A on/off		15 / 0		V
	SKHI 22B on/off		5 / 0		V
V_{iT+}	Input threshold voltage (High) SKHI 22A	10,9	11,7	12,5	V
	SKHI 22B	3,5	3,7	3,9	V
V_{iT-}	Input threshold voltage (Low) SKHI 22A	4,7	5,5	6,5	V
	SKHI 22B	1,5	1,75	2,0	V
R_{in}	Input resistance SKHI 22A		10		kΩ
	SKHI 22B		3,3		kΩ
$V_{G(on)}$	Turn on gate voltage output		+ 15		V
$V_{G(off)}$	Turn off gate voltage output		- 7		V
R_{GE}	Internal gate-emitter resistance		22		kΩ
f_{ASIC}	Asic system switching frequency		8		MHz
$t_{d(on)IO}$	Input-output turn-on propagation time	0,85	1	1,15	µs
$t_{d(off)IO}$	Input-output turn-off propagation time	0,85	1	1,15	µs
$t_{d(err)}$	Error input-output propagation time		0,6		µs
$t_{pERRRESET}$	Error reset time		9		µs
t_{TD}	Top-Bot Interlock Dead Time SKHI 22A	3,3		4,3	µs
	SKHI 22B	no interlock		4,3	µs
V_{CEsat}	Reference voltage for V_{CE}-monitoring		5[2)]	10	V
C_{ps}	Coupling capacitance primary secondary		12		pF
MTBF	Mean Time Between Failure T_a = 40°C		2,0		10^6 h
w	weight		45		g

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